ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT (AITAM) TEKKALI

(Approved by AICTE, Accredited by NBA Affiliated to JNTU, Kakinada)

STUDENT ATTENDENCE REGISTER

Name	: MATTA MANI SANKAR
Subject	: STLD (EEE Dept.)
Class	: II - C
Year	: 2014-15

Scanned by CamScanner

LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
1	1/9/14	Introduction to Digital electronics	UNIT I	class Room		
2	2/9/14	Advantages of digital ckts, sequential, combinational ckts	UNIT I	class Room		
3	4/9/14	Review of whole course	unit-I	class Room		
4	5/9	Review of Number systems	UNIT-I	CR		
5	8/9	Binary No. system, converting in Binary	UNIT-I	CR		
6	8/9	Conversion b/w bases	UNIT-I	CR		
7	9/9	Conversion b/w bases	UNIT-I	CR		
8	12/9	R's & R-1's compliments Binary Arthmetic	UNIT-I	CR		
9	12/9	codes, 8421 BCD	UNIT-I	CR		
10	15/9	8421 BCD, XS-3, Gray code	UNIT-I	CR		
11.	16/9	Parity, Block parity Hamming	UNIT-I	CR		
12.	18/9	Hamming, 2421 BCD	UNIT-I	CR		
13.	19/9	Binary arithmetic	UNIT-I	CR		
14.	22/9	Logic Gates, AND, OR, NOT, NAND, NOR,	UNIT-II	CR		
15.	23/9	Universal gates realisation	UNIT-II	CR		
16.	26/9	Boolean Theorems & minimization	UNIT-II	CR		
17	26/9	Standard SOP and standard POS	UNIT-II	CR		
18.	6/10	Complements & Duals.	II	CR		
19.	27/10	Multilevel NAND-NAND, NOR-NOR	II	CR		
20.	28/10	NAND-NAND, NOR-NOR	II	CR		

Scanned by CamScanner

LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
21 31/10	31/10	Universal Gates	II	CR		
31/10 32	31/10	K - Map - 2 variables	III	CR		
22.	3/11	3 variables, 4 variables	III	CR		
24.	4/11	don't cares & 5 variable	III	CR		
25.	7/11	Example problems on K-maps	III	CR		
26.	7/11	Code converters	III	CR		
27.	10/11	Binary multipliers	III	CR		
28.	11/11	Tabular minimization	III	CR		
29.	14/11	Tabular minimization	III	CR		
30.	14/11	Half adder, full adder	IV	CR		
31.	17/11	Half subtractor, full subtractor	IV	CR		
32.	18/11	4-bit adder	IV	CR		
33	21/11	Look ahead adder	IV	CR		
34	21/11	adder sub ckt	IV	CR		
35	24/11	BCD adders, MUX	IV	CR		
36.	25/11	DeMUX, Encoder	IV	CR		
37	28/11	Decoders, priority encoder	IV	CR		
38	28/11	7-segment display	IV	CR		
39	1/12	combinational logic design MUX	IV	CR		
40	2/12	Latch, FF	V	CR		

Scanned by CamScanner

LESSON PLAN

Period	Date (tentative)	Topic	Unit No	Teaching Methodology	Remarks	Corrective Action Upon Review
41	8/11	SR FF, JKFF	IV	CR		
42	9/11	Excitation table, state diagram	IV	CR		
43	11/11	Triggering Mechanisms	IV	CR		
44	12/11	Flipflop conversions	IV	CR		
45	15/11	Counters, Ripple counters	IV	CR		
46	16/11	Synchronous counters	IV	CR		
47	17/11	Johnson counters	IV	CR		
48	19/11	Ring counters	IV	CR		
49	22/11	Registers, buffer type	IV	CR		
50	23/11	Shift, Control Buffer	IV	CR		
51	26/11	Bidirectional Register	IV	CR		
52	29/11	Universal Register	IV	CR		

Scanned by CamScanner