ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT (AITAM) TEKKALI

(Approved by AICTE, Accredited by NBA Affiliated to JNTU, Kakinada)

STUDENT ATTENDENCE REGISTER

Name : .....

Subject : .....

Class : .....

Year : .....

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LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
4	8/9/14	Introduction	1	Class Room		
2	9/9/14	Review of Number system	1	"		
6	10/9/14	Types of Number system	1	"		
5	10/9/14	Bax conversion methods Complements	1	"		
2	15/9/14	Complement subtraction & introduction to codes	1	"		
5	16/9/14	8-4-2-1, 2421, Excess-3 Self complement codes	1	"		
6	16/9/14	gray code, error detection & Correction codes	1	"		
5	17/9/14	Introduction to logic Gates NOT, AND, OR, NAND, NOR, EX-OR, EX-NOR	2	"		
2	22/9/14	Logic Gates truth tables	2	"		
5	23/9/14	Boolean theorems & proofs.	2	"		
6	23/9/14	Complement & dual of logic expressions	2	"		
5	24/9/14	Standard SOP & Standard POS.	2	"		
2	29/9/14	Minimization of logic functions using theorems	2	"		
5	7/10/14	Implementation Logic gates using NAND & NOR	2	"		
6	7/10/14	Ex-NOR & EX-OR gates Implement using NAND & NOR	2	"		
5	8/10/14	Multi-level NAND-NAND Implementation	2	"		
2	27/10/14	Multi-level NOR-NOR Implementation.	2	"		
5	28/10/14	Minimization of Switching function using K-Map	3	"		
6	28/10/14	Minimization of switching functions using K-Map	3	"		
5	29/10/14	Minimization of switching functions using K-Map	3	"		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
2	3/11/14	Code converters	3	Classroom		
5	4/11/14	binary Multiplier using K-Map	3	"		
6	4/11/14	Tabular Minimization	3	"		
5	5/11/14	Minimization techniques using tabular method	3	"		
2	10/11/14	Review of 3rd unit	3	"		
5	11/11/14	Review of K-map & Variable terminals	3	"		
6	11/11/14	Review of 3rd unit	3	"		
5	12/11/14	Introduction to Combinational logic circuits	4	"		
2	17/11/14	Half adder & full adder	4	"		
5	18/11/14	Half subtractor & full subtractor	4	"		
6	18/11/14	Application of full adder 4-bit binary adder	4	"		
5	19/11/14	4-bit binary Subtractor	4	"		
2	24/11/14	Adder - Subtractor circuit	4	"		
5	25/11/14	BCD adder circuit	4	"		
6	25/11/14	Excess-3 adder circuit	4	"		
5	26/11/14	look-a-head adder circuit	4	"		
2	2/12/14	Design of decoder	4	"		
5	8/12/14	Design of Encoder	4	"		
6	8/12/14	Design of Multiplexer	4	"		
2	8/12/14	Design of Multiplexer	4	"		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
5	9/12/14	Design of demultiplexer	4	class Room		
6	9/12/14	Design of demultiplexer	4	"		
5	10/12/14	Design of Multiplexer	4	"		
2	15/12/14	Design of Demultiplexer	4	"		
5	16/12/14	Priority Encoder	4	"		
6	16/12/14	Comparator	4	"		
5	17/12/14	Seven segment display	4	"		
2	22/12/14	Review of 4th unit	4	"		
5	23/12/14	Review of 4th unit	4	"		
6	23/12/14	Introduction to sequential logic circuits.	5	"		
5	24/12/14	flip-flops with truth tables	5	"		
2	29/12/14	flip-flops with truth tables	5	"		
5	30/12/14	Flip-flops with excitation tables	5	"		
6	30/12/14	Flip-flop with excitation tables	5	"		
5	31/12/14	Conversion of Flip-flop to Flip-flop	5	"		
2	5/01/15	Conversion of Flip-flop to Flip-flop	5	"		
5	6/01/15	Conversion of Flip-flop to Flip-flop	5	"		
6	6/01/15	Design of ripple Counters	5	"		
5	7/01/15	Design of Synchronous Counters	5	"		
2	12/1/15	Johnson Counter	5	"		

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LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
5	13/1/15	Ring Counters	5	Classroom		
5	10/1/15	Design of all counters	5	"		
6	10/1/15	Design of Buffer register	5	"		
6	13/1/15	Control buffer register	5	"		
6	13/1/15	Shift register	5	"		
5	14/1/15	bi-directional shift register	5	"		
5	14/1/15	Universal shift register	5	"		

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