**LESSON PLAN**

**Branch**: III ECE 'B' **Semester**: I **Subject** : DICA

**Acadamic year: 2015-16** **faculty :Swathi jallu**

| Period | Date (Tentative) | Topic | Unit No. | Teaching Methodology | Remarks | Corrective Action upon Review |
|---|---|---|---|---|---|---|
| | | **Logic Families** | I | | | |
| 1. | 22.07.2015 | Introduction to CMOS logic | I | Black Board | | |
| 2. | 23.07.2015 | CMOS logic levels | I | B.B | | |
| 3. | 24.07.2015 | CMOS logic gates | I | B.B | | |
| 4. | 29.07.2015 | CMOS steady state electrical behavior | I | B.B | | |
| 5. | 30.07.2015 | CMOS dynamic electrical behavior | I | B.B | | |
| 6. | 30.07.2015 | CMOS logic families. | I | B.B | | |
| 7. | 31.07.2015 | Bipolar logic, diode Logic | I | B.B | | |
| 8. | 05.08.2015 | Transistor logic | I | B.B | | |
| 9. | 06.08.2015 | logic families | | | | |
| 10. | 06.08.2015 | TTL logic families | I | B.B | | |
| 11. | 07.08.2015 | CMOS/TTL interfacing, | I | B.B | | |
| 12. | 12.08.2015 | Low voltage CMOS logic and interfacing | I | B.B | | |
| 13. | 12.08.2015 | Emitter coupled logic, comparison of logic families. | I | B.B | | |
| | 13.08.2015 | **Combinational Logic Design – I** | II | | | |
| 14. | 14.08.2015 | Introduction | | B.B | | |
| 15. | 15.08.2015 | Design and analysis procedures of decoders | II | B.B | | |
| 16. | 15.08.2015 | Design and analysis procedures of encoders, | II | B.B | | |
| 17. | 19.08.2015 | Three state devices, | II | B.B | | |
| 18. | 20.08.2015 | multiplexers and de-multiplexers, | II | B.B | | |
| 19. | 20.08.2015 | EX-OR gates | II | B.B | | |
| 20. | 21.08.2015 | Parity circuits | II | B.B | | |
| 21. | 21.08.2015 | Comparators. | II | B.B | | |
| 22. | 02.09.2015 | Design considerations of the above combinational logic with relevant digital ICs. | II | B.B | | |
| 23. | 02.09.2015 | VHDL modeling of decoders, encoders, multiplexers and comparators. | II | B.B | | |

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| | | **Combinational Logic Design–II** | III | | | |
| 24. | 03.09.2015 | Introduction | III | B.B | | |
| 25. | 04.09.2015 | Design and analysis procedures of adders | III | B.B | | |
| 26. | 09.09.2015 | Subtractors | III | B.B | | |
| 27. | 10.09.2015 | ALUs | III | B.B | | |
| 28. | 10.09.2015 | Barrel shifter, | III | B.B | | |
| 29. | 11.09.2015 | Simple floating-point encoder | III | B.B | | |
| 30. | 11.09.2015 | Dual parity encoder | III | B.B | | |
| 31. | 16.09.2015 | Cascading of comparators | III | B.B | | |
| 32. | 17.09.2015 | Combinational multipliers. | III | B.B | | |
| 33. | 17.09.2015 | Design considerations of the above combinational logic with relevant digital ICs. | III | B.B | | |
| 34. | 18.09.2015 | VHDL modeling of adders, Subtractors, barrel shifter and combinational multipliers | III | B.B | | |
| 35. | 23.09.2015 | VHDL modeling of barrel shifter and combinational multipliers | III | B.B | | |
| | | **Sequential Logic Design** | IV | | | |
| 36. | 23.09.2015 | Introduction | IV | B.B | | |
| 37. | 24.09.2015 | Latches | IV | B.B | | |
| 38. | 24.09.2015 | Flip-flops | IV | B.B | | |
| 39. | 25.09.2015 | Counters | IV | B.B | | |
| 40. | 07.10.2015 | Shift registers | IV | B.B | | |
| 41. | 08.10.2015 | synchronous design methodology, | IV | B.B | | |
| 42. | 08.10.2015 | Impediments to synchronous design. | IV | B.B | | |
| 43. | 09.10.2015 | VHDL modeling of ripple counters, | IV | B.B | | |
| 44. | 14.10.2015 | VHDL modeling of synchronous counters | IV | B.B | | |
| 45. | 15.10.2015 | VHDL modeling of Shift Registers | IV | B.B | | |
| | | **PLD** | V | | | |
| 46. | 16.10.2015 | Introduction to PROM | V | B.B | | |
| 47. | 21.10.2015 | RAM | V | B.B | | |
| 48. | 28.10.2015 | PLA, PAL | V | B.B | | |
| 49. | 29.10.2015 | CPLD | V | B.B | | |
| 50. | 30.10.2015 | FPGA | V | B.B | | |
| 51. | 04.11.2015 | Design considerations of PLDs. | V | B.B | | |
| 52. | 04.11.2015 | relevant digital ICs | | B.B | | |
| 53. | 05.11.2015 | VHDL modeling of memories and PLDs. | V | B.B | | |
| 54. | 05.11.2015 | Revision | V | B.B | | |

**TEXT BOOKS** :


1. Digital Design Principles & Practices – John F. Wakerly, PHI/ Pearson Education Asia, 2005, 3/e.
2. Digital IC Applications – Atul P.Godse and Deepali A.Godse, Technical Publications, Pune, 2005.
3. VHDL Primer – J. Bhasker, PHI,3rd Edition.


**Reference books:**


1. Digital System Design Using VHDL – Charles H. Roth Jr., PWS Publications,1998.
2. Digital Logic and Computer Design by Morris Mano, Prentice Hall.