LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
1,	20/07/15	Logic families	I	Black Board		
2,	20/07/15	Introduction to		"		
	"	CMOS logic				
3,	21/07/15	CMOS logic levels		"		
4,	22/07/15	Gates using CMOS logic		"		
5,	23/07/15	CMOS Steady State		"		
		electrical behaviour				
6,	29/07/15	CMOS dynamic		"		
		Electrical behaviour				
7,	30/07/15	CMOS logic families		"		
8,	06/08/15	Bipolar logic		"		
		Diode logic				
9,	06/08/15	Transistor logic		"		
10,	10/08/15	TTL logic families		"		
11,	13/08/15	CMOS/TTL Interfacing		"		
12,	13/08/15	Low voltage CMOS		"		
		logic & Interfacing				
13,	14/08/15	Emitter Coupled logic		"		
14,	17/08/15	comparision of		"		
		logic families				

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
15	11/08/15	Introduction	II	BB/CB		
		combinational				
		logic Design - I				
16	10/08	Decoder design &		"		
		Analysis				
17	14/08/15	Encoder Design &		"		
		Analysis				
18	15/08/15	Three State Device		"		
		Design & Analysis				
19	03/09/15	MUX, DEMUX		"		
		design & Analysis				
20	07/09/15	X-OR Gates		"		
21	7/09/15	Parity circuits		"		
22	08/09/15	Comparators		"		
23	09/09/15	Design consideration		"		
		with Relevant-				
		digital IC's				
24	14/09/15	VHDL modeling of		"		
		decoder, Encoder				
25	15/09/15	Multiplexer, Comparator		"		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
26	15/09/15	combinational logic	III	Black Board		
		Design & Analysis				
27	18/09/15	Procedures of Adders		"		
28	18/09/15	Subtractors,		"		
		ALU's				
29	21/09/15	Barrel Shifter		"		
		floating Point encoder				
30	23/09/15	Dual Parity Encoder		"		
31	24/09/15	encoding comparator		"		
32	24/09/15	Combinational		"		
		Multipliers				
33	27/09/15	Design considerations		"		
		with digital IC's				
34	29/09/15	VHDL modelling of		"		
		Adders, Subtractor				
35	05/10/15	Barrel Shifters, Multipliers		"		
		sequential logic	IV	"		
36	05/10/15	Design & Introduction				
37	13/10/15	Latches	I	"		
38	08/10/15	Flipflops		"		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
39	10/10/15	Counters		Black Board		
40	12/10/15	Shift Registers		"		
41	12/10/15	Synchronous Design		"		
		Methodology				
42	14/10/15	Impediments to Design		"		
43	15/10/15	VHDL Modeling to		"		
44	16/10/15	Ripple counters		"		
45	17/10/15	Shift Registers		"		
46	19/10/15	Synchronous counters		"		
47	20/10/15	Introduction to PLD's	V	"		
48	24/10/15	PROM, RAM		"		
49 50	24/10/15 ~~23/10/15~~	PAL, PLA		"		
51	27/10/15	CPLD		"		
52	02/11/15	FPGA		"		
53	02/11/15	Design consideration of		"		
54	03/11/15	PLDs with Digital IC		"		
55	04/11/15	VHDL modeling		"		
		of memories				
56	06/11/15	VHDL modeling of PLDs		"		
		Revision		"		