LESSON PLAN

Subject Code & Name: 13EC3013 & DIGITAL IC APPLICATIONS **Branch: ECE**
Class / Semester: III B.Tech I Semester ECE 'A' **Academic Year: 2015-16**

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks
		Unit-1 Logic Families			
1.	**20.07.2015**	logic families	**1**	**BB & Chalk**	
2.	**21.07.2015**	Introduction	**1**	**BB & Chalk**	
3.	**21.07.2015**	CMOS logic	**1**	**BB & Chalk**	
4.	**24.07.2015**	CMOS logic levels	**1**	**BB & Chalk**	
5.	**27.07.2015**	Gates using CMOS	**1**	**BB & Chalk**	
6.	**28.07.2015**	CMOS steady state electrical behavior	**1**	**BB & Chalk**	
7.	**28.07.2015**	CMOS dynamic electrical behavior	**1**	**BB & Chalk**	
8.	**31.07.2015**	CMOS logic families	**1**	**BB & Chalk**	
9.	**03.08.2015**	bipolar logic, diode Logic	**1**	**BB & Chalk**	
10.	**04.08.2015**	Transistor logic, TTL families	**1**	**BB & Chalk**	
11.	**04.08.2015**	CMOS/TTL interfacing,	**1**	**BB & Chalk**	
12.	**07.08.2015**	low voltage CMOS logic and interfacing	**1**	**BB & Chalk**	
13.	**10.08.2015**	emitter coupled logic	**1**	**BB & Chalk**	
14.	**11.08.2015**	comparison of logic families	**1**	**BB & Chalk**	
		Unit-2 Combinational Logic Design – I			
15.	**11.08.2015**	Introduction	**2**	**BB & Chalk / LCD**	
16.	**14.08.2015**	Combinational logic design	**2**	**BB & Chalk / LCD**	
17.	**17.08.2015**	Design and analysis procedures of decoders	**2**	**BB & Chalk**	
18.	**18.08.2015**	Design and analysis procedures of encoders,	**2**	**BB & Chalk /LCD**	
19.	**18.08.2015**	Three state devices,	**2**	**BB & Chalk**	
20.	**21.08.2015**	multiplexers	**2**	**BB & Chalk**	
21.	**24.08.2015**	de-multiplexers, EX-OR gates.	**2**	**BB & Chalk**	
22.	**25.08.2015**	parity circuits and comparators	**2**	**BB & Chalk**	
23.	**25.08.2015**	Design considerations of the above combinational logic with relevant digital ICs.	**2**	**BB & Chalk**	
24.	**31.08.2015**	VHDL modeling of decoders, encoders	**2**	**BB & Chalk**	
25.	**01.09.2015**	VHDL modeling of multiplexers & comparators.	**2**	**BB & Chalk**	
		UNIT-III Combinational Logic Design – II			
26.	**01.09.2015**	Design and analysis procedures	**3**	**BB & Chalk /LCD**	
27.	**04.09.2015**	adders	**3**	**BB & Chalk /LCD**	
28.	**07.09.2015**	Subtractors, ALUs	**3**	**BB & Chalk /LCD**	
29.	**08.09.2015**	barrel shifter, simple floating-point encoder,	**3**	**BB & Chalk /LCD**	
30.	**08.09.2015**	dual parity encoder,	**3**	**BB & Chalk /LCD**	
31.	**11.09.2015**	cascading comparators	**3**	**BB & Chalk**	
32.	**14.09.2015**	Combinational multipliers	**3**	**BB & Chalk**	
33.	**15.09.2015**	Design considerations of the above combinational logic	**3**	**BB & Chalk**	

		with relevant digital ICs.			
34.	**18.09.2015**	VHDL modeling of adders, subtractors,	**3**	**BB & Chalk**	
35.	**22.09.2015**	barrel shifter, combinational multipliers	**3**	**BB & Chalk**	
		Unit-4 **Sequential Logic Design**			
36.	**22.09.2015**	Introduction	**4**	**BB & Chalk**	
37.	**25.09.2015**	Sequential Logic Design	**4**	**BB & Chalk**	
38.	**05.10.2015**	Latches	**4**	**BB & Chalk /LCD**	
39.	**06.10.2015**	flip-flops	**4**	**BB & Chalk /LCD**	
40.	**06.10.2015**	Counters	**4**	**BB & Chalk**	
41.	**09.10.2015**	shift registers	**4**	**BB & Chalk**	
42.	**12.10.2015**	synchronous design methodology	**4**	**BB & Chalk**	
43.	**13.10.2015**	Impediments to synchronous design.	**4**	**BB & Chalk**	
44.	**13.10.2015**	VHDL modeling of ripple counters,	**4**	**BB & Chalk**	
45.	**16.10.2015**	synchronous counters			
46.	**26.10.2015**	shift registers			
		Unit-5 **PLDs**			
47.	**27.10.2015**	Introduction to PLDs	**5**	**BB & Chalk**	
48.	**27.10.2015**	PROM, RAM	**5**	**BB & Chalk /LCD**	
49.	**30.10.2015**	PLA	**5**	**BB & Chalk /LCD**	
50.	**02.11.2015**	PAL	**5**	**BB & Chalk /LCD**	
51.	**03.11.2015**	CPLD	**5**	**BB & Chalk /LCD**	
52.	**03.11.2015**	FPGA	**5**	**BB & Chalk /LCD**	
53.	**04.11.2015**	Design considerations of PLDs with relevant digital ICs.	**5**	**BB & Chalk**	
54.	**06.11.2015**	Design considerations of PLDs with relevant digital ICs.	**5**	**BB & Chalk**	
55.	**09.11.2015**	VHDL modeling of memories	**5**	**BB & Chalk**	
56.	**10.11.2015**	VHDL modeling of PLDs	**5**	**BB & Chalk**	
57.	**10.11.2015**	Revision	**5**	**BB & Chalk**	

Faculty Name:

III ECE-A : Smt. E.Jaya III ECE-B: Smt. J. Swathi III ECE-C : Sri S. umamaheswara rao

CR: CLASS ROOM BB: BLACK BOARD OHP: OVERHEAD PROJECTOR LCD

Text books:

1. Digital Design Principles & Practices – John F. Wakerly, PHI/ Pearson Education Asia, 2005, 3/e.
2. Digital IC Applications – Atul P.Godse and Deepali A.Godse, Technical Publications, Pune, 2005.
3. VHDL Primer – J. Bhasker, PHI,3rd Edition.

Reference books:

1. Digital System Design Using VHDL – Charles H. Roth Jr., PWS Publications,1998.
2. Digital Logic and Computer Design by Morris Mano, Prentice Hall.

FACULTY FACULTY IN-CHARGE HEAD OF THE DEPARTMENT