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LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
(1)	20/1/15	Introduction	I	BB		
(2)	20/1/15	IC technologies	I	"		
		Comparasion Moores law etc.				
(3)	22/1/15	Basic MOS transistor dep.	I	"		
(4)	22/1/15	Enhancement mode operation	I	"		
(5)	23/1/15	IC production process N-MOS fabrication P-MOS fabrication	I	"		
(6)	23/1/15	CMOS fabrication	I	"		
(7)	27/1/15	Bicmos technology discussion	I	"		
(8)	29/1/15	comparasion of various IC technologies	I	"		
(9)	29/1/15	I_{ds} Vs V_{ds} relationship	II	"		
(10)	31/1/15	Aspects of MOS transistor threshold voltage	II	"		
(11)	3/2/15	MOS transistor transconductance conductance cut-off figure of merit	II	BB		
(12)	3/2/15	pass transistor, N-MOS inverter	II	BB		
(13)	5/2/15	pull up to pull down ratio	II	BB		
(14)	5/2/15	problem on pull up to pull down ratio with two pass transistors	II	BB		

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15	9/2/15	Alternative form of pull-up	II	BB		
(16)	10/2/15	CMOS Inverter				
(17)	10/2/15	BiCMOS Inverter	II	BB		
(18)	12/2/15	Latch-up in BiCMOS-CMOS	II	BB		
		and latch-up susceptibility				
(19)	12/2/15	Mask layout & stick diagrams	III	BB		
(20)	13/2/15	Stick diagrams continued	III	BB		
(21)	13/2/15	Design rules of layout	III	BB		
(22)	17/2/15	Standard CMOS & poly wires	III	BB		
		wires				
(23)	19/2/15	CMOS/BiCMOS wires	III	BB		
(24)	20/2/15	Metal, poly contacts	III	BB		
(25)	24/2/15	Layout diagrams of NAND, NOR	III	BB		
(26)	24/2/15	Layout diagrams for CMOS	III	BB		
(27)	26/2/15	Symbolic Diagrams - Translation to layout form	III	BB		
(28)	27/2/15	Sheet resistance, applied to	IV	BB		
		MOS transistors				
(29)	3/3/15	Sheet Resistance applied to inverters	IV	BB		
(30)	4/3/15	Area capacitance of layers and	IV	BB		
		standard unit of capacitance				

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
(31)	5/8/15	Area capacitance Calculations delay unit	IV	BB		
(32)	5/8/15	Inverter delays	IV	BB		
(33)	6/8/15	Driving large capacitance loads	IV	BB		
(34)	10/8/15	propagation delays wiring capacitance	IV	BB		
(35)	10/8/15	fanin fanout choice of layers transistors	IV	BB		
(36)	12/8/15	realization of gates using nmos, pmos, cmos	IV	BB		
(37)	14/8/15	Scaling of mos transistors models and factors device parameters	V	BB		
(38)	17/8/15	Scaling out used	V	BB		
(39)	19/8/15	Limitations of Scaling Scaling due to current density	V	BB		
(40)	19/8/15	device supply voltages,	V	BB		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
(41)	20/3/15	Architecture levels.	V	BB		
(42)	23/3/15	Introduction to Switch logic and Gate logic	V	BB		
(43)	23/3/15	Introduction to PLDs	VI	BB		
(44)	24/3/15	PAL, PLA with Implementation	VI	BB		
(45)	24/3/15	Implementation approaches in VLSI design	VI	BB		
(46)	28/3/15	Full custom design	VI	BB		
(47)	31/3/15	Semi custom design	V	BB		
(48)	31/3/15	Gate array & standard cell	VI	BB		
(49)	2/4/15	CPLDs	VI	BB		
(50)	2/4/15	FPGAs, Design flows	VI	BB		
(51)	3/4/15	Digital system design process	VII	BB		
(52)	7/4/15	VLSI CKT design process.	VII	BB		
(53)	7/4/15	HDL Simulation, Synthesis	VII	BB		
(54)	9/4/15	Introduction to VHDL	VII	BB		
(55)	9/4/15	Requirements, abstraction, Elements of VHDL	VII	BB		
(56)	10/4/15	Libraries, objects and classes,	VII	BB		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
68	30/4/15	Revision of		BB		
		Concept - V, VI		BB		
69	30/4/15	Revision of -		BB		
		VII, VIII				
70	1/5/15	Discussion of -		BB		
		previous yr QP paper				Qs Paper