LESSON PLAN

od	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Act Upon Revie
0	7/1/16	R-2R based converter		Board		
1	8/1/16	Thermometer code current mode D/A Converters		"		
2	18/1/16	Integrating Converter		"		
63	19/1/16	Successive approximation Converter		"		
64	20/1/16	DAC based Successive approximation		"		
65	21/1/16	Flash Converter		"		
66	22/1/16	Time interleaved A/D converter		"		
				Board		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Upon Re
47	16/12/15	XC 9500 CPLD architecture		Board		
	17/12/15			"		
48	18/12/15	CLB internal architecture		"		
				"		
49	21/12/15	I/O block internal architecture		"		
				"		
50	22/12/15	FPGA		"		
51	23/12/15	CLB, I/O architecture		"		
	24/12/15			"		
52	28/12/15	Comparators	VI	Board		
53	29/12/15	latched comparators		"		
54	30/12/15	Decoder based Converter		"		
55	31/12/15	Resistor string Converter		"		
56	1/1/16	folded resistor string Converter		"		
57	4/1/16	Binary scale Converter		"		
58	5/1/16	Binary weighted resistor Converters		"		
59	6/1/16	Reduced resistance		"		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Correct Upon
31	23/12/15	logic families & characteristics	IV	Board		
32	24/12/15	Interfacing comparison of logic families		"		
33	25/12/15	comparators		"		
34	26/12/15	VHDL modelling for decoders, Encoders		"		
35	28/12/15	Mux, comparator		"		
36	29/12/15	adders & Subtractor		"		
37	1/1/16	VHDL modelling for latches, flip-flops		"		
	2/1/16					
38	3/1/16	Counter, shift register		"		
39	4/1/16	FSM, ASM Charts		"		
40	7/1/16	Problems		"		
41	8/1/16	MUX & decoders	V	Board		
42	9/1/16	Barrel shifter, Counter		"		
43	10/1/16	digital Simple bit adder		"		
44	11/1/16	ROM internal structure		"		
45	14/1/16	2D decoding		"		
46	15/1/16	RAM internal structure		"		

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Period	Date (Planned)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
[illegible]	[illegible]	Problems	[illegible]	Board		
[illegible]	[illegible]	Basic op amp	III	Board		
	[illegible]	capacitor switches		"		
[illegible]	[illegible]	[illegible]		"		
[illegible]	[illegible]	Operation & Analysis		"		
	[illegible]	of resistor equivalent of a switched capacitor		"		
21	[illegible]	Parasitic sensitive		"		
	[illegible]	integrator, parasitic		"		
22	[illegible]	insensitive integrators		"		
23	2/11/15	Signal flow graph analysis		"		
				"		
24	3/11/15	first order filter		"		
25	4/11/15	switch sharing		"		
	5/11/15	fully differential filters		"		
26	6/11/15	switched capacitor gain circuits		"		
27	9/11/15	Parallel resistor capacitor circuit		"		
28	10/11/15	Other switched capacitors		"		
29	11/11/15	full wave rectifier		"		

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks
1	21/9/15	unit-I General consideration	I	Board	
		of one stage op-amp		"	
2	22/9/15	Two stage op-amp		"	
3	23/9/15	Gain boosting stage		"	
4	24/9/15	Comparision i/p range limitations slew rate		"	
5	28/9/15	Basic current mirror Circuit		"	
6	29/9/15	cascode, wilsons current mirror circuit		"	
7	29/9/15	CS, CG Amplifiers		"	
8	30/9/15	Types of noise		"	
9	1/10/15	Noise in common source stage noise bandwidth		"	
10	2/10/15	Problems			
11	5/10/15	unit-II PLL Concept	II	Board	
12	6/10/15	PLL in locked condition		"	
13	7/10/15	IC - PLL's		"	
14	8/10/15	Phase detector		"	
15	9/10/15	Voltage controlled oscillator		"	
16	12/10/15	Case study: Analysis of monolithic		"	