LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
		UNIT - II		Black board & PPT's		
49	28/12/15	Parwan CPU (Introduction)	II	"		
50	29/12/15					
51	04/01/16	Behavioural Description of Parwan	II	"		
52	05/01/16	Running Structure	II	"		
52	09/01/16	Data flow description test bench for the Parwan CPU	II	"		
53	19/01/16	Realistic PARWAN CPU	II	"		
54	21/01/16	Interface design and modeling	II	"		
55	22/01/16	VHDL as a modeling language	II	"		

	Date	Topics	Unit No.	Teaching Methodology	Remarks	
				Black board & PPTs		
		User defined Attributes	4			
		Packaging Basic utilities	4	"		
		Unit - 5				
		Multiplexing and Data selection	5	"		
		State Machine Descriptions	5	"		
		Open collector gates	5	"		
		Three state Buffers	5	"		
		A general Data flow circuit				
		Updating Basic utilities	5	"		
		Behavioural description of hardware	5	"		
		Process statement vs various statements	5	"		
		Sequential circuit Statements (various forms)	5	"		
		Parameterized Models & operators	5	"		
		Test Bench design	5	"		

LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Acti Upon Revie
		Unit - 3		Black board & PPT's		
17.	19/10/15	Definition and Usage of	3	"		
18	20/10/15	Subprograms	3	"		
19.	26/10/15	Packaging parts	3	"		
20	27/10/15	& Utilities				
21.	29/10/15	Design Parame-	3	"		
22	30/10/15	terization				
23	02/11/15	Design	3	"		
	03/11/15	Configuration		"		
24	05/11/15	Design Libraries	3	"		
25	06/11/15					
		Unit - 4				
26.	09/11/15	Utilities for high-level description	4	"		
27.	10/11/15	Type Declaration & Usage	4	"		
28	12/11/15	VHDL Operators	4	"		
29	13/11/15	Sub program parameter types	4	"		
		and overloading		"		
30.	23/11/15	other types & type related	4	"		
31.	24/11/15	issues				
	26/11/15	Predefined Attribu-	4	"		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
		Unit - 1				
1.	21/09/15	An overview of design procedures used	1	Blackboard & PPTs		
		for System Design using CAD tools	1	"		
2.	22/09/15	Design Entry & Synthesis	1	"		
3.	24/09/15	Simulation, Optimization, Place & Route	1	"		
4.	25/09/15	Design Verification tools	1	"		
5.	28/09/15	Elements of VHDL	1	"		
6.	29/09/15	Top Down Design with VHDL Subprograms	1	"		
7.	01/10/15	Controller description in VHDL	1	"		
8.	02/10/15	VHDL Operators	1	"		
		Unit - 2				
9.	05/10/15	Characterizing hardware Languages	2	"		
10.	06/10/15	Objects & Classes	2	"		
11.	08/10/15	Signal Assignments	2	"		
12.	09/10/15	Concurrent & Sequential Assignments	2	"		
13.	12/10/15	Parts Library wiring of Primitives	2	"		
14.	13/10/15	wiring Interactive networks	2	"		
15	15/10/15	Modeling a test Bench	2	"		
16.	16/10/15	Binding Alternative Top Down Wiring	2	"		