

**ACADEMIC REGULATIONS
COURSE STRUCTURE AND SYLLABI
FOR
M.TECH**

VLSI System Design

(Department of Electronics and Communication Engineering)

From The Academic Year 2013-2014



ADITYA Institute of Technology And Management
(AUTONOMOUS)

Approved by AICTE, Permanently Affiliated to JNTUK, Kakinada
Accredited by NBA & NAAC, Recognised by UGC under 2(f) & 12(b)

K Kotturu, TEKKALI, Srikakulam Dist., A.P

VISION

To evolve into a premier engineering institute in the country by continuously enhancing the range of our competencies, expanding the gamut of our activities and extending the frontiers of our operations.

MISSION

Synergizing knowledge, technology and human resource, we impart the best quality education in Technology and Management. In the process, we make education more objective so that the efficiency for employability increases on a continued basis.

Academic Regulations 2013 for M.Tech (Regular)

(With effect from batch admitted in the academic year 2013-2014)

The M.Tech Degree of the Aditya Institute of Technology and Management (Autonomous), Tekkali shall be conferred on candidates who are admitted to the programme and fulfill all the requirements for the award of the Degree.

1. ELIGIBILITY FOR ADMISSIONS:

Admission to the above programme shall be made subject to the eligibility, qualifications and specialization prescribed by the University from time to time. Admissions shall be made on the basis of merit rank obtained by the qualifying candidate in GATE / PG CET, subject to reservations prescribed by the Govt. of AP from time to time.

2. AWARD OF M. Tech DEGREE:

- 2.1** A student shall be declared eligible for award of the M.Tech degree, if he/she pursues a course of study and completes it successfully in not less than two academic years and not more than four consecutive academic years and registered for **80** credits and he/she must secure total **80** credits.
- 2.2** A student, who fails to fulfill all the academic requirements for the award of the degree within four academic years from the year of his/her admission, shall forfeit his/her seat in M.Tech course.
- 2.3** The minimum clear instruction days for each semester are 95.

3. ATTENDANCE:

- 3.1** A candidate shall be deemed to have eligibility to write End Semester examinations if he/she has put in a minimum of 75% of attendance in aggregate of all the subjects.
- 3.2** Condonation of shortage of attendance up to 10% (65% and above, and below 75%) may be given by the College academic committee.
- 3.3** Condonation of shortage of attendance shall be granted only on genuine and valid reasons on representations by the candidate with supporting evidence.
- 3.4** Shortage of attendance below 65% shall in NO case be condoned.

- 3.5** A candidate shall not be promoted to the next semester unless he/she fulfills the attendance requirements of the present semester.
- 3.6** A stipulated fee shall be payable towards condonation of shortage of attendance.

4. COURSE OF STUDY:

The following specializations are offered at present for the M.Tech course of study.

| | |
|---|---|
| 1 | Digital Electronics and Communication Systems |
| 2 | VLSI System Design |
| 3 | Power Electronics and Electric Drives |
| 4 | Computer Science and Engineering |
| 5 | Information Technology |
| 6 | Thermal Engineering |

5. EVALUATION:

The performance of the candidate in each semester shall be evaluated subject-wise, with a Maximum of 100 marks for theory and 100 marks for Laboratory, on the basis of Internal Evaluation and End Semester Examination.

- 5.1** For the theory subjects 60 marks shall be awarded based on the performance in the End Semester Examination. Out of 40 internal marks **30** marks are assigned for subjective exam, 5 marks for subjective assignments and 5 marks for seminars. The internal evaluation for 30 marks shall be made based on the **average** of the marks secured in the two Mid Term-Examinations conducted, one in the middle of the Semester and the other immediately after the completion of instruction. Each midterm examination shall be conducted in a duration of 120 minutes and question paper shall contain **4** questions. The student should answer all **4** questions.

- 5.2** For practical subjects, 60 marks shall be awarded based on the performance in the End Semester Examinations. Out of 40 internal marks 20 marks are assigned based on day to day evaluation and 20 marks are assigned based on the internal test.
- 5.3** There shall be a technical seminar presentation during 3rd semester. For technical seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the Department in a report form and shall make an oral presentation before the Departmental Committee. The Departmental Committee consists of Head of the Department, supervisor and two other senior faculty members of the department. For technical seminar there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% to be declared successful.
- 5.4** A candidate shall be deemed to have secured the academic requirement in a subject if he/she secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.
- 5.5** In case the candidate does not secure the minimum academic requirement in any Subject (as specified in 5.4) he has to reappear for the supplementary Examination in that subject.
- 5.6** The viva-voce examination shall be conducted at the end of the course work and after the candidate passing all subjects.
- 5.7** Laboratory examination for M.Tech courses must be conducted with two Examiners, one of them being Laboratory Class Teacher and second examiner shall be external examiner.

6. EVALUATION OF PROJECT/DISSERTATION WORK:

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the Project Review Committee.

- 6.1** A Project Review Committee (PRC) shall be constituted with Principal as chair person, Head of the department, one senior faculty member and project guide.

- 6.2** Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects (theory and practical).
- 6.3** After satisfying 6.2, a candidate has to submit, in consultation with his / her project supervisor, the title, objective and plan of action of his project work (Based on a publication in a Peer Reviewed Journal) to the Project Review Committee for its approval before the second semester end examinations. After obtaining the approval of the Committee, the student can initiate the Project work after the second semester end examinations.
- 6.4** Every candidate shall work on projects approved by the PRC of the college.
- 6.5** If a candidate wishes to change his supervisor or topic of the project, he/she can do so with approval of the PRC. However, the Project Review Committee (PRC) shall examine whether the change of topic/supervisor leads to a major change of his initial plans of project proposal. If so, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.
- 6.6** A candidate shall submit status report in two stages at least with a gap of 3 months between them.
- 6.7** The work on the project shall be initiated in the beginning of the second year/III semester and minimum duration of the project is two semesters. The candidate shall identify the problem, Literature survey, design/modeling part of the problem i.e. almost 35% of his dissertation/project work should complete in the III semester itself and it will be evaluated by PRC. If the candidate fails to get the satisfactory report, he has to re-register for the project/dissertation work.
- 6.8** A candidate shall be allowed to submit the project report only after fulfilling the attendance requirements of all the semesters with approval of PRC and not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Principal (through Head of the Department) and shall make an oral presentation before the PRC.
- 6.9** The Candidate may be permitted to submit the Project Report, if only after the work is Published/Accepted to be Published in a Journal / International conference of repute and relevance.

- 6.10** Three copies of the Project Thesis certified by the supervisor shall be submitted to the College/Institute.
- 6.11** The thesis shall be adjudicated by external examiner from outside the college.
- 6.12** The viva-voce examination shall be conducted by a board consisting of the supervisor, Head of the Department and the examiner outside the college who adjudicated the Thesis.
- 6.13** The student has to clear all the subjects of M.Tech course before submission of the project thesis/ dissertation

The Board shall jointly report candidates work as :

- A. Excellent
- B. Good
- C. Satisfactory
- D. Unsatisfactory

Head of the Department shall coordinate and make arrangements for the conduct of viva-voce examination. If the report of the viva-voce is unsatisfactory, the candidate has to retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second viva-voce examination, the candidate may be asked to submit a new project proposal to PRC starting with 6.5

7. METHOD OF AWARDING LETTER GRADES AND GRADE POINTS FOR A COURSE.

A letter grade and grade points will be awarded to a student in each course based on his/her performance as per the grading system given below.

Table: Grading System for M.Tech. Programme

| Percentage of Marks | Grade Points | Letter Grade |
|---------------------|--------------|--------------|
| 90-100 | 10 | S |
| 80-89 | 9 | A |
| 70-79 | 8 | B |
| 60-69 | 7 | C |
| 50-59 | 6 | D |
| 40-49 | 5 | E |
| < 40 | 0 | F (Fail) |

7.1 Calculation of Semester Grade Points Average (SGPA)* for semester

The performance of each student at the end of the each semester is indicated in terms of SGPA. The SGPA is calculated as below:

$$\text{SGPA} = \frac{\Sigma(\text{CR} \times \text{GP})}{\Sigma \text{CR}} \quad (\text{for all courses passed in semester})$$

Where CR = Credits of a Course

GP = Grade points awarded for a course

*SGPA is calculated for the candidates who passed all the courses in that semester.

7.1.1 Calculation of Cumulative Grade Points Average (CGPA) and Award of Division for Entire Programme.

The CGPA is calculated as below:

$$\text{CGPA} = \frac{\Sigma(\text{CR} \times \text{GP})}{\Sigma \text{CR}} \quad (\text{for entire programme})$$

Where CR = Credits of a course

GP = Grade points awarded for a course

Table: Award of Divisions

| CGPA | DIVISION |
|----------------|------------------------------|
| ≥ 8 | First Class with distinction |
| $\geq 7 - < 8$ | First Class |
| $\geq 6 - < 7$ | Second Class |
| < 6 | Fail |

After a student has satisfied the requirements prescribed for the completion of the programme and is eligible for receiving the award of M.Tech. Degree, he shall be placed in one of the above three divisions.

8. WITH-HOLDING OF RESULTS:

If the candidate has not paid any dues to the college or if any case of indiscipline is pending against him / her, the result of the candidate will be withheld and he/she will not be allowed into the next higher semester. The issue of the degree is liable to be withheld in such cases.

9. TRANSITORY REGULATIONS:

Candidate who have discontinued or have been detained for want of attendance or who have failed after having undergone the course are eligible for admission to the same or equivalent subjects as and when subjects are offered, subject to 5.5 and 2.0

10. GENERAL:

- 10.1** The academic regulations should be read as a whole for purpose of any Interpretation.
- 10.2** In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Principal is final.
- 10.3** The Institute may change or amend the academic regulations and syllabus at any time and the changes and amendments made shall be applicable to all the students with effect from the date notified by the college.
- 10.4** Wherever the word he, him or his occur, it will also include she, her and hers.

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M.TECH COURSE STRUCTURE

| M. Tech. (VLSI System Design) – 1 st SEMESTER | | | | | | | |
|--|----------------------|------------------------------------|-----------|---|-----------|------------|-----|
| S. No. | Sub. Code | SUBJECT | L | P | C | INT | EXT |
| 1 | 13MVL1001 | Digital System Design | 4 | - | 3 | 40 | 60 |
| 2 | 13MVL1002 | VLSI Technology & Design | 4 | - | 3 | 40 | 60 |
| 3 | 13MVL1003 | Analog & Digital IC Design | 4 | - | 3 | 40 | 60 |
| 4 | 13MVL1004 | VHDL Modeling of Digital Systems | 4 | - | 3 | 40 | 60 |
| 5 | Elective – I | | 4 | - | 3 | 40 | 60 |
| | 13MVL1005 | Digital Data Communications | | | | | |
| | 13MVL1006 | Embedded & Real Time Systems | | | | | |
| 6 | Elective – II | | 4 | - | 3 | 40 | 60 |
| | 13MVL1007 | Electronic Design Automation Tools | | | | | |
| | 13MVL1008 | VLSI Signal Processing | | | | | |
| 7 | 13MVL1101 | HDL Programming Laboratory | - | 4 | 2 | 40 | 60 |
| TOTAL | | | 28 | | 20 | 700 | |

| M. Tech. (VLSI System Design) – 2 nd SEMESTER | | | | | | | |
|---|-----------------------|---|-----------|---|-----------|------------|-----|
| S. No. | Sub. Code | SUBJECT | L | P | C | INT | EXT |
| 1 | 13MVL1009 | DSP Processors and architecture | 4 | - | 3 | 40 | 60 |
| 2 | 13MVL1010 | Algorithms for VLSI Design Automation | 4 | - | 3 | 40 | 60 |
| 3 | 13MVL1011 | Low Power VLSI Design | 4 | - | 3 | 40 | 60 |
| 4 | 13MVL1012 | Design of Fault Tolerant Systems | 4 | - | 3 | 40 | 60 |
| 5 | Elective – III | | 4 | - | 3 | 40 | 60 |
| | 13MVL1013 | System Modeling & Simulation | | | | | |
| | 13MVL1014 | MOS devices modeling | | | | | |
| 6 | Elective – IV | | 4 | - | 3 | 40 | 60 |
| | 13MVL1015 | CPLD and FPGA Architecture and Applications | | | | | |
| | 13MVL1016 | Network Security and Cryptography | | | | | |
| 7 | 13MVL1102 | Mixed Signal simulation Lab | - | 4 | 2 | 40 | 60 |
| TOTAL | | | 28 | | 20 | 700 | |

| M. Tech. (VLSI System Design) – 3 rd SEMESTER | | | | | | | |
|---|-----------|----------------------|----------|---|-----------|------------|-----|
| S. No. | Sub. Code | SUBJECT | L | P | C | INT | EXT |
| 1 | 13MVL2201 | Technical Seminar | - | - | 2 | 100 | - |
| 2 | 13MVL2202 | Project Work Phase-1 | - | - | 18 | - | - |
| TOTAL | | | - | | 20 | 100 | |

| M. Tech. (VLSI System Design) – 4 th SEMESTER | | | | | | | |
|---|-----------|----------------------|----------|---|-----------|----------|-----|
| S. No. | Sub. Code | SUBJECT | L | P | C | INT | EXT |
| 1 | 13MVL2203 | Project Work Phase-2 | - | - | 20 | - | - |
| TOTAL | | | - | | 20 | - | |

L – Lecture hours/Week; P – Practical hours/ Week; C – Credits; INT – Internal Marks;
EXT – External Marks;

DIGITAL SYSTEM DESIGN

(Common to VLSI and DECS)

SUBJECT CODE: 13MVL1001

| L | P | C | INT | EXT |
|---|---|---|-----|-----|
| 4 | 0 | 3 | 40 | 60 |

COURSE OBJECTIVES:

- The main objective of this course is to introduce concepts and designing principles of various digital systems used in designing of digital circuits.

COURSE OUTCOMES:

- Able to understand the concept and designing of various digital systems.
- Acquire knowledge in the testing of designed digital systems.

UNIT – I

DESIGN OF DIGITAL SYSTEMS:

ASM charts, Hardware description language and control sequence method, Reduction of state tables, State assignments.

UNIT – II

SEQUENTIAL CIRCUIT DESIGN:

Design of Iterative circuits, Design of sequential circuits using ROMs and PLAs, Sequential circuit design using CPLD, FPGAs.

UNIT – III

FAULT MODELING:

Fault classes and models – Stuck at faults, bridging faults, transition and intermittent faults.

FAULT DIAGNOSIS IN SEQUENTIAL CIRCUITS:

State identification and fault detection experiment. Machine identification, Design of fault detection experiment.

UNIT – IV

TEST GENERATION:

Fault diagnosis of Combinational circuits by conventional methods – Path Sensitization technique, Boolean difference method, Kohavi algorithm.

TEST PATTERN GENERATION:

D – algorithm, PODEM, Random testing, transition count testing, Signature analysis and testing for bridging faults.

UNIT – V**PROGRAMMING LOGIC ARRAYS:**

Design using PLA's, PLA minimization and PLA folding.

PLA TESTING:

Fault models, Test generation and Testable PLA design.

UNIT – VI**ASYNCHRONOUS SEQUENTIAL MACHINE:**

fundamental mode model, flow table, state reduction, minimal closed covers, races, cycles and hazards.

TEXT BOOKS:

1. Z. Kohavi – “Switching & finite Automata Theory” (TMH).
2. N. N. Biswas – “Logic Design Theory” (PHI).
3. N. Balabanian, Bradley Calson – “Digital Logic Design Principles” – Wiley Student Edition 2004.

REFERENCE BOOKS:

1. M. Abramovici, M. A. Breues, A. D. Friedman – “Digital System Testing and Testable Design”, Jaico Publications.
2. Charles H. Roth Jr. – “Fundamentals of Logic Design”.
3. Frederick. J. Hill & Peterson – “Computer Aided Logic Design” – Wiley 4th Edition.

VLSI TECHNOLOGY & DESIGN

(Common to VLSI and DECS)

SUBJECT CODE: 13MVL1002

| L | P | C | INT | EXT |
|---|---|---|-----|-----|
| 4 | 0 | 3 | 40 | 60 |

COURSE OBJECTIVES:

- The main objective of this course is to introduce basic concepts of microelectronics, layout designing, floor planning and algorithms used in the chip designing process.

COURSE OUTCOMES:

- Student is able to understand the concepts of and electrical properties of MOS technologies.
- Student is able to understand different types layout designing tools and floor planning methods used in chip design.
- Student is able to design combinational logic networks and sequential systems.
- Student is able to understand CAD algorithms used in chip design.

UNIT – I

REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS

TECHNOLOGIES:

(MOS, CMOS, Bi CMOS) Technology trends and projections. Lithography, Oxidation, Ion implantation, Metalization and Diffusion techniques.

BASIC ELECTRICAL PROPERTIES OF MOS, CMOS & BICOMS CIRCUITS:

Ids-Vds relationships, Threshold voltage V_t , G_m , G_{ds} and W_o , Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Z_{pu}/Z_{pd} , MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT – II

LAYOUT DESIGN AND TOOLS:

Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

LOGIC GATES & LAYOUTS: Static complementary gates, switch logic, Alternative gate circuits, low power gates, Resistive and Inductive interconnect delays.

UNIT – III

COMBINATIONAL LOGIC NETWORKS:

Layouts, Simulation, Network delay, interconnect design, power optimization, Switch logic networks, Gate and Network testing.

UNIT – IV

SEQUENTIAL SYSTEMS:

Memory cells and Arrays, clocking disciplines, System Design, power optimization, Design validation and testing.

UNIT – V

FLOOR PLANNING & ARCHITECTURE DESIGN:

Floor planning methods, off-chip connections, High-level synthesis, Architecture for low power, SOCs and Embedded CPUs, Architecture testing.

UNIT – VI

INTRODUCTION TO CAD SYSTEMS (ALGORITHMS) AND CHIP DESIGN:

Layout Synthesis and Analysis, Scheduling and printing, Hardware/Software Co-design, chip design methodologies- A simple Design example.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian et. al (3 authors) PHI of India Ltd.,2005.
2. Modern VLSI Design, 3rd Edition, Wayne Wolf, Pearson Education, 5th Indian Reprint, 2005.

REFERENCE BOOKS:

1. Principals of CMOS Design – N.H.E Weste, K.Eshraghian, Adison Wesley, 2nd Edition.
2. Introduction to VLSI Design – Fabricius, MGH International Edition, 1990.
3. CMOS Circuit Design, Layout and Simulation – Baker, Li Boyce, PHI, 2004.
4. VLSI Technology - 2nd Edn.- S.M.Sze.

ANALOG AND DIGITAL IC DESIGN

(Common to VLSI and DECS)

SUBJECT CODE:13MVL1003

| L | P | C | INT | EXT |
|---|---|---|-----|-----|
| 4 | 0 | 3 | 40 | 60 |

COURSE OBJECTIVES:

- The course provides understanding the main principles of various analog and digital building blocks used in IC design.

COURSE OUTCOMES:

- Able to understand the concepts analog building blocks like operational amplifier, phase locked loops and switched capacitors.
- Able to understand the concepts and designing of digital building blocks like combinational logic circuits, sequential logic circuits using VHDL.

UNIT – I

OPERATIONAL AMPLIFIERS:

General considerations one – state op-amps, two stage op-amps-gains boosting stage-comparison I/P range limitations slew rate.

CURRENT MIRRORS AND SINGLE STAGE AMPLIFIERS:

Simple COMS, BJT current mirror, Cascode Wilson Wilder current mirrors. Common Source amplifier source follower, common gate amplifier

NOISE: Types of Noise – Thermal Noise-flicker noise- Noise in opamps- Noise in common source stage noise band width.

UNIT – II

PHASED LOCKED LOOP DESIGN:

PLL concepts- The phase locked loop in the locked condition Integrated circuit PLLs – phase Detector- Voltage controlled oscillator case study: Analysis of the 560 B Monolithic PLL.

UNIT – III

SWITCHED CAPACITORS CIRCUITS:

Basic Building blocks op-amps capacitors switches – non-over lapping clocks-Basic operations and analysis-resistor equivalence of 1a switched capacitor- parasitic sensitive integrator parasitic insensitive integrators signal flow graph analysis-First order filters- switch sharing fully differential filters – charged injections-switched capacitor gain circuits parallel resistor –capacitor circuit – preset table gain circuit – other switched capacitor circuits – full wave rectifier – peak detector sinusoidal oscillator.

UNIT – IV

LOGIC FAMILIES & CHARACTERISTICS:

COMS, TTL, ECL, logic families COMS/ TTL, interfacing comparison of logic families.

COMBINATIONAL LOGIC DESIGN USING VHDL:

VHDL modeling for decoders, encoders, multiplexers, comparison, adders and subtractors.

SEQUENTIAL IC DESIGN USING VHDL:

VHDL modeling for latches, flip flaps, counters, shift registers FSMs. ASM charts.

UNIT – V

DIGITAL INTEGRATED SYSTEM BUILDING BLOCKS:

Multiplexers and decoders – barrel shifters counters digital single bit adder.

MEMORIES:

ROM Internal structure, 2D decoding commercial type timing and applications, RAM internal structure.

CPLD:

XC 9500 series family CPLD architecture – CLB internal architecture, I/O block internal structure.

FPGA:

Conceptual of view of FPGA – classification based on CLB internal architecture I/O block architecture.

UNIT – VI**COMPARATORS:**

Using an op-amp for a comparator-charge injection errors- latched comparator.

NYQUIST RATE D/A CONVERTERS:

Decoder based converter resistor string converters folded resistor string converter – Binary scale converters – Binary weighted resistor converters – Reduced resistance ratio ladders – R-2R based converters – Thermometer code current mode D/A converters.

NYQUIST RATE A/D CONVERTERS:

Integrating converters – successive approximation converters. DAC based successive approximation – flash converters time interleaved A/D converters.

TEXT BOOKS:

1. Analog Integrated circuit Design by David A Johns, Ken Martin, John Wiley & Sons.
2. Analysis and design of Analog Integrated Circuits, by Gray, Hurst Lewis, Meyer. John Wiley & Sons.
3. Design of Analog CMOS Integrated Circuits, Behzad Razavi, TMH
4. Digital Integrated Circuit Design by Ken Martin, Oxford University 2000
5. Digital Design Principles & Practices” by John F Wakerly, Pearson Education & Xilinx Design Series, 3rd Ed.(2002)

REFERENCE BOOKS:

1. Ken Martin, Digital Integrated Circuit Design Oxford University, 2000.
2. John F Wakerly, “Digital Design Principles & Practices”, Pearson Education & Xilinx Design Series, 3rd Ed.(2002)
3. Samir Palnitkar, “Verylog HDL-A Guide to Digital Design and Synthesis”, Prentice Hall India, (2002)
4. Douglas J Smith, “HDL Chip Design, a practical Guide for Designing, Synthesizing and simulating ASICs and FPGAs

VHDL MODELING OF DIGITAL SYSTEMS

SUBJECT CODE: 13MVL1004

| L | P | C | INT | EXT |
|---|---|---|-----|-----|
| 4 | 0 | 3 | 40 | 60 |

COURSE OBJECTIVES:

- The main objective of this course is to introduce basic concept of modeling of different digital systems using VHDL.

COURSE OUTCOMES:

- Able to understand the concept of modeling digital circuits using VHDL.
- Acquire knowledge in design organization, parameterization and CPU modeling of digital components using VHDL.

UNIT – I

INTRODUCTION:

An Overview Of Design Procedures Used For System Design Using CAD Tools. Design Entry. Synthesis, Simulation, Optimization, Place and Route. Design Verification Tools. Examples Using Commercial PC Based On VHDL Elements Of VHDL, Top Down Design With VHDL Subprograms. Controller Description VHDL Operators.

UNIT – II

BASIC CONCEPT IN VHDL:

Characterizing Hardware Languages, Objects And Classes, Signal Assignments, Concurrent And Sequential Assignments. Structural Specification Of Hardware: Parts Library Wiring Of Primitives, Wiring Interactive Networks, Modeling A Test Bench Binding Alternative Top Down Wiring.

UNIT – III

DESIGN ORGANIZATIN AND PARAMETERIZATION – 1:

Definition And Usage If Subprograms, Packaging Parts And Utilities, Design Parameterization, Design Configuration, Design Libraries.

UNIT – IV

DESIGN ORGANIZATIN AND PARAMETERIZATION – 2:

Utilities For High –Level Descriptions-Type Declaration And Usage, VHDL Operators, Subprogram Parameter Types And Overloading, Other Types And Type Related Issues, Predefined Attributes, User Defined Attributes, Packing Basic Utilities.

UNIT – V

DATA FLOW DESCRIPTION IN VHDL:

Multiplexing And Data Selection, State Machine Description, Open Collector Gates, Three State Bussing A General Data Flow Circuit, Updating Basic Utilities. Behavioral Description Of Hardware: Process Statement As section Statements, Sequential Wait Statements Formatted ASCII I/O Operators, MSI-Based Design.

UNIT – VI

CPU MODELLING FOR DESCRIPTION IN VHDL:

Parwan CPU, Behavioral Description of Parawan, Bussing Structure, Data Flow Description Test Bench for the Parwan CPU. A More Realistic Parwan. Interface Design And Modeling.VHDL As A Modeling Language.

TEXT BOOK:

1. Z.NAWABI: VHDL Analysis And Modeling Of Digital Systems. (2/E), McGraw Hill,(1998)

REFERENCE BOOK:

1. PERRY: VHDL, (3/E) McGraw Hill 10

DIGITAL DATA COMMUNICATIONS

(Common to VLSI and DECS)(Elective-1)

SUBJECT CODE: 13MVL1005

| L | P | C | INT | EXT |
|----------|----------|----------|------------|------------|
| 4 | 0 | 3 | 40 | 60 |

COURSE OBJECTIVES:

- The main objective of this course is to introduce basic concepts of various methods used in transmitting digital data using wired and wireless communication.

COURSE OUTCOMES:

- Student is able to understand different types of digital modulation techniques.
- Student is able to understand the concepts of digital multiplexing, local area networks and multimedia.
- Student is able to understand various interfaces and methods used to transmit digital data.

UNIT – I

DIGITAL MODULATION TECHNIQUES:

FSK, MSK, BPSK, QPSK, 8-PSK, 16-PSK, 8- QAM, 16 - QAM, Band width efficiency carrier recovery DPSK, clock recovery, Probability of error and bit error rate.

UNIT – II

DATA COMMUNICATIONS:

Serial, Parallel configuration, Topology, Transmission modes, codes, Error Control Synchronization, LCU.

UNIT – III

Serial and Parallel Interfaces, Telephone Networks and Circuits and data modems.

Data Communication Protocols, Character and block Mode, Asynchronous and Synchronous Protocols, public Data Networks, ISDN.

UNIT – IV

DIGITAL MULTIPLEXING:

TDM, T1 carrier, CCITT, CODECS, COMBO CHIPS, North American Hierarchy, Line Encoding, T-carrier, Frame Synchronization Inter Leaving Statistical TDM FDM , Hierarchy ,Wave Division Multiplexing .

UNIT – V

LOCAL AREA NETWORKS:

Token ring, Ethernet, Traditional, Fast and GIGA bit Ethernet, FDDI.

WIRELESS LANS IEEE 802.11:

Architecture Layers, Addressing, Blue Tooth Architecture Layers, 12 Cap, Other Upper Layers.

UNIT – VI

MULTI MEDIA:

Digitalizing Video and Audio Compression Streaming Stored and Live Video and Audio, Real Time Interactive Video and Audio, VOIP.

TEXT BOOKS:

1. Electronic communication systems, fundamentals through advanced - W. TOMASI, Pearson 4th Edition.
2. Data communication and networking - B.A. Forouzen

EMBEDDED AND REAL TIME SYSTEMS

(Common to VLSI and DECS)(Elective-1)

SUBJECT CODE: 13MVL1006

| L | P | C | INT | EXT |
|---|---|---|-----|-----|
| 4 | 0 | 3 | 40 | 60 |

COURSE OBJECTIVES:

- To introduce the basic concepts of embedded systems.
- To clearly differentiate the different issues that arises in designing soft and hard real-time systems.
- To explain the various concepts of time that arises in real-time systems.

COURSE OUTCOMES:

- The student got familiarity with design of embedded systems.
- Master the core knowledge of real-time embedded system design.
- Develop skills for application of core knowledge.

UNIT – I

INTRODUCTION:

Embedded systems over view, design challenges, processor technology, Design technology, Trade-offs. Single purpose processors RT-level combinational logic, sequential logic(RTlevel), custom purpose processor design(RT -level), optimizing custom single purpose processors.

GENERAL PURPOSE PROCESSORS:

Basic architecture, operations, programmer's view, development environment, Application specific Instruction –Set processors (ASIPs)-Micro controllers and Digital signal processors.

UNIT – II

STATE MACHINE AND CONCURRENT PROCESS MODELS:

Introduction, models Vs Languages, finite state machines with data path model(FSMD),using state machines, program state machine model(PSM, concurrent process model, concurrent processes, communication among

processes, synchronization among processes, Implementation, data flow model, real-time systems.

UNIT – III

COMMUNICATION PROCESSES:

Need for communication interfaces, RS232/UART, RS422/RS485,USB, Infrared, IEEE1394 Firewire, Ethernet, IEEE 802.11, Blue tooth.

UNIT – IV

EMBEDDED/RTOS CONCEPTS-I:

Architecture of the Kernel, Tasks and task scheduler, interrupt service routines, Semaphores, Mutex.

EMBEDDED/RTOS CONCEPTS -II &:

Mailboxes, Message Queues, Event Registers, Pipes-Signals.

UNIT – V

EMBEDDED/RTOS CONCEPTS –III:

Timers-Memory Management-Priority inversion problem embedded operating systems-Embedded Linux-Real-time operating systems-RT Linux-Handheld operating systems-Windows CE.

UNIT – VI

DESIGN TECHNOLOGY:

Introduction, Automation, Synthesis, parallel evolution of compilation and synthesis, Logic synthesis, RT synthesis, Behavioral Synthesis, Systems Synthesis and Hardware/Software Co-Design, Verification, Hardware/Software co-simulation, Reuse of intellectual property codes.

TEXT BOOKS:

1. Embedded System Design-A Unified Hardware/Software Introduction- Frank Vahid, Tony D. Givargis, John Wiley & Sons, Inc.2002.
2. Embedded/Real Time Systems- KVKK prased, Dreamtech press-2005.
3. Introduction to Embedded Systems - Raj Kamal, TMS-2002.

REFERENCE BOOKS:

1. Embedded Microcomputer Systems-Jonathan W.Valvano,
Books/Cole,Thomson Leaarning.
2. An Embedded Software Primer- David E.Simon, pearson Ed.2000

ELECTRONIC DESIGN AUTOMATION TOOLS

(Elective-II)

SUBJECT CODE: 13MVL1007

| L | P | C | INT | EXT |
|----------|----------|----------|------------|------------|
| 4 | 0 | 3 | 40 | 60 |

COURSE OBJECTIVES:

- The course provides basic understanding the concepts, synthesis and simulation of digital systems using verilog and PSPICE and PCB layout design.

COURSE OUTCOMES:

- Able to understand the concept of design and simulation of digital systems using Verilog.
- Able to understand the concept of design and simulation of digital systems using PSPICE. Able to design and analyze PCB layouts.

UNIT – I

IMPORTANT CONCEPTS IN VERILOG:

Basics of Verilog Language, Operators, Hierarchy, Procedures And Assignments, Timing Controls And Delay. Tasks And Functions Control Statements, Logic-Gate Modeling, Modeling Delay, Altering Parameters, And Other Verilog Features.

UNIT – II

SYNTHESIS AND SIMULATION USING HDLS – 1:

Verilog and Logic Synthesis. VHDL And Logic Synthesis, Memory Synthesis, FSM Synthesis, Memory Synthesis, Performance-Driven Synthesis. Simulation-Types Of Simulation, Logic Systems Working Of Logic Simulation.

UNIT – III

SYNTHESIS AND SIMULATION USING HDLS – 2:

Cell Models, Delay Models State Timing Analysis, Formal Verification, Switch-Level Simulation Transistor-Level Simulation. CAD Tools For Synthesis And Simulation Modelism And Leonardo Spectrum (Exemplar).

UNIT – IV

TOOLS FOR CIRCUIT DESIGN AND SIMULATION USING PSPICE:

Pspice Models For Transistors, A/D & D/A Sample And Hold Circuits Etc, And Digital System Building Blocks, Design And Analysis Of Analog And Digital Circuits Using PSPICE.

UNIT – V

AN OVER VIEW OF MIXED SIGNAL VLSI DESIGN:

Fundamentals Of Analog And Digital Simulation, Mixed Signal Simulator Configurations, Understanding Modeling, Integration To CAE Environments, Analyses Of Analog Circuits Eg. A/D, D/A Converters, Up And Down Converters, Compounders Etc.

UNIT – VI

TOOLS FOR PCB DESIGN AND LAYOUT:

An Overview of High Speed PCB Design, Design Entry, Simulation And Layout Tools For PCB. Introduction To Orcad PCB Design Tools.

TEXTBOOKS:

1. J.Bhaskar, A Verilog Primer, BSP, 2003. 2. J.Bhaskar, A Verilog HDL Synthesis BSP, 2003. 3. M.H.RASHID: SPICE FOR Circuits And Electronics Using PSPICE (2/E)(1992) Prentice Hall.

REFERENCE BOOK:

1. ORCAD: Technical Reference Manual, Orcad, USA. 2. SABER: Technical Reference Manual, Analogic Nic, USA.

VLSI SIGNAL PROCESSING

(Elective-II)

SUBJECT CODE: 13MVL1008

| L | P | C | INT | EXT |
|---|---|---|-----|-----|
| 4 | 0 | 3 | 40 | 60 |

COURSE OBJECTIVES:

- The objective of this course is to teach students about the designing of digital signal processors in VLSI.

COURSE OUTCOMES:

- Upon completion of this course, students will understand the architectural requirements of DSP processors and how to implement the DSP architectures in VLSI.

UNIT – I

INTRODUCTION TO DSP:

Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms. Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power, Retiming: Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques

UNIT – II

FOLDING:

Introduction - Folding Transform – Register minimization Techniques – Register minimization in folded architectures – folding of multirate systems.

UNIT – III

UNFOLDING: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding.

UNIT – IV

SYSTOLIC ARCHITECTURE DESIGN:

Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain delays.

UNIT – V

FAST CONVOLUTION:

Introduction – Cook-Toom Algorithm – Winograd algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

UNIT – VI

LOW POWER DESIGN:

Scaling Vs Power Consumption –Power Analysis, Power Reduction techniques – Power Estimation Approaches.

PROGRAMMABLE DSP:

Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing.

TEXT BOOKS:

1. Keshab K. Parthi, VLSI Digital Signal Processing- System Design and Implementation –1998, Wiley Inter Science.
2. Kung S. Y, H. J. White House, T. Kailath, VLSI and Modern Signal processing, 1985, Prentice Hall.
3. Jose E. France, Yannis Tsividis, Design of Analog – Digital VLSI Circuits for telecommunications and Signal Processing –1994, Prentice Hall.
4. Mediseti V. K ,VLSI Digital Signal Processing , IEEE Press (NY), USA, 1995.

HDL PROGRAMMING LABORATORY

(Common to VLSI and DECS)

SUBJECT CODE: 13MVL1101

| L | P | C | INT | EXT |
|----------|----------|----------|------------|------------|
| 0 | 4 | 2 | 40 | 60 |

COURSE OBJECTIVES:

- To develop, analyze and experience with principle of designing digital circuits.

COURSE OUTCOMES:

- The students can simulate, synthesis and implement the digital circuits by using VHDL/Verilog and FPGA/CPGA devices.

Students are required to simulate, synthesize and implement the following experimental part, on the VHDL/Verilog environment.

1. Digital Circuits Description using Verilog and VHDL
2. Verification of the Functionality of Designed circuits using function Simulator.
3. Timing simulation for critical path time calculation.
4. Synthesis of Digital circuits
5. Place and Route techniques for major FPGA vendors such as Xilinx, Altera and Actel etc.
6. Implementation of Designed Digital Circuits using FPGA and CPLD devices.

DSP PROCESSORS AND ARCHITECTURES

(Common to VLSI and DECS)

SUBJECT CODE: 13MVL1009

| L | P | C | INT | EXT |
|----------|----------|----------|------------|------------|
| 4 | 0 | 3 | 40 | 60 |

COURSE OBJECTIVES:

- To have an overview of digital signal processing.
- To study the design of various building blocks of DSP processors.
- To study the designing of programmable DSP processors.

COURSE OUTCOMES:

- At the end of the course, the student will be able to:
- Understand required building blocks to design a DSP processors.
- Understand different DSP processors and basic programming skills.

UNIT – I

INTRODUCTION TO DIGITAL SIGNAL PROCESING:

Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.

UNIT – II

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS:

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT – III

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES:

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation

Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

EXECUTION CONTROL AND PIPELINING:

Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT – IV

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS:

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT – V

IMPLEMENTATIONS OF BASIC DSP AND FFT ALGORITHMS:

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

UNIT – VI

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES:

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP

Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS:

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. S. Chand & Co, 2000.

REFERENCE BOOKS:

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkata Ramani and M. Bhaskar, TMH, 2004.
2. Digital Signal Processing – Jonatham Stein, John Wiley, 2005

ALGORITHMS FOR VLSI DESIGN AUTOMATION

SUBJECT CODE: 13MVL1010

| L | P | C | INT | EXT |
|---|---|---|-----|-----|
| 4 | 0 | 3 | 40 | 60 |

COURSE OBJECTIVES:

- To explain the various algorithms used to design VLSI in automation.
- To study the various optimization techniques in the process of automation.

COURSE OUTCOMES:

- Ability to model automation of VLSI design.
- Ability to apply optimization techniques to the process of VLSI design.

UNIT – I

PRELIMINARIES:

Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational Complexity, Tractable and Intractable Problems.

UNIT – II

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION:

Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT – III

Layout Compaction, Placement, Floor planning and Routing Problems, Concepts and Algorithms

MODELING AND SIMULATION:

Gate Level Modeling and Simulation, Switch level Modeling and simulation.

UNIT – IV

LOGIC SYNTHESIS AND VERIFICATION:

Basic issues and Terminology, Binary –Decision diagram, Two – Level Logic Synthesis.

HIGH LEVEL SYNTHESIS:

Hardware Models, Internal representation of the input algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High – level Transformations.

UNIT – V

PHYSICAL DESIGN AUTOMATION OF FPGA’S:

FPGA technologies, Physical Design cycle for FPGA’s partitioning and Routing for segmented and staggered models.

UNIT – VI

PHYSICAL DESIGN AUTOMATION OF MCM’S:

MCM technologies, MCM physical design cycle, Partitioning, Placement – Chip array based and full custom approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, routing and programmable MCM’s

TEXT BOOKS:

1. Algorithms for VLSI Design Automation, S.H.Gerez, WILEY student edition, John wiley & Sons (Asia) Pvt.Ltd. 1999.
2. Algorithms for VLSI Physical Design Automation, 3rd edition, Naveed Sherwani, Springer International Edition, 2005

REFERENCE BOOKS:

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, Wiley, 1993
2. Modern VLSI Design: Systems on silicon – Wavne Wolf, Pearson Education Asia, 2nd Edition, 1998

LOW POWER VLSI DESIGN

SUBJECT CODE: 13MVL1011

| L | P | C | INT | EXT |
|---|---|---|-----|-----|
| 4 | 0 | 3 | 40 | 60 |

COURSE OBJECTIVES:

- To familiarize the students with the different types of low power design methods/models used in VLSI design.

COURSE OUTCOMES:

- After completing the course, the students will be able to understand in detail the need and use of low power devices in the design of VLSI.

UNIT – I

LOW POWER DESIGN AN OVER VIEW:

Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

MOS/BiCMOS PROCESSES:

Bi CMOS processes, Integration and Isolation considerations, Integrated, Analog/Digital CMOS Process.

UNIT – II

LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES:

Deep submicron processes ,SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/BiCMOS processes.

UNIT – III

DEVICE BEHAVIOR AND MODELING:

Advanced MOSFET models, limitations of MOSFET models, Bipolar models.

UNIT – IV

Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybridmode environment.

UNIT – V

LOW- VOLTAGE LOW POWER LOGIC CIRCUITS:

Comparison of advanced BiCMOS Digital circuits. ESD-free Bi CMOS, Digital circuit operation and comparative Evaluation.

UNIT – VI

CMOS AND Bi-CMOS LOGIC GATES:

Conventional CMOS and BiCMOS logic gates, Performance Evaluation.

LOW POWER LATCHES AND FLIP FLOPS:

Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

TEXT BOOKS:

1. CMOS/BiCMOS ULSI low voltage, low power by Yeo Rofail/ Gohl(3 Authors)- Pearson Education Asia 1st Indian reprint,2002

REFERENCE BOOKS:

1. Digital Integrated circuits, J.Rabaey PH. N.J 1996
2. CMOS Digital ICs sung-moKang and yusuf leblebici 3rd edition TMH2003 (chapter 11)
3. VLSI DSP systems, Parhi, John Wiley & sons, 2003 (chapter 17)
4. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and InternationalConferences and Symposia.

DESIGN OF FAULT TOLERANT SYSTEMS

SUBJECT CODE: 13MVL1012

| L | P | C | INT | EXT |
|---|---|---|-----|-----|
| 4 | 0 | 3 | 40 | 60 |

COURSE OBJECTIVES:

- To explain the various faults occurred in VLSI design and methods of checking and safe design of overcome the faults.

COURSE OUTCOMES:

- Students will have good understanding of the basic faults occurred in VLSI design.
- Students will understand the methods to test, checking and safe design to overcome the faults in VLSI design.

UNIT – I

BASIC CONCEPTS:

Reliability concepts, Failure & Faults, Reliability and failure rate, Relation between reliability and meantime between failure, Maintainability and Availability, Reliability of series, Parallel and Parallel-Series combinational circuits.

UNIT – II

FAULT TOLERANT DESIGN:

Basic concepts – Static, dynamic, hybrid, Triple Modular Redundant System, Self purging redundancy, Siftout redundancy (SMR), SMR Configuration, Use of error correcting code, Time redundancy and software redundancy.

UNIT – III

SELF CHECKING CIRCUITS:

Basic concepts of Self checking circuits, Design of Totally Self Checking checker, Checkers using m out of n codes, Berger code, Low cost residue code.

UNIT – IV

FAIL SAFE DESIGN:

Strongly fault secure circuits, fail-safe design of sequential circuits using partition theory and Berger code, totally self-checking PLA design.

UNIT – V

DESIGN FOR TESTABILITY FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS:

Basic concepts of testability, controllability and observability, the Reed Muller's expansion technique, OR-AND-OR design, use of control and syndrome testable design. Controllability and observability by means of scan register Storage cells for scan design, classic scan design, Level Sensitive Scan Design (LSSD).

UNIT – VI

Theory and operation of LFSR, LFSR as Signature analyzer, Multiple-input Signature Register.

BUILT IN SELF TEST:

BIST concepts, Test pattern generation for BIST exhaustive testing, Pseudorandom testing, pseudo exhaustive testing, constant weight patterns, Generic offline BIST architecture.

TEXT BOOKS:

1. Parag K. Lala – “Fault Tolerant & Fault Testable Hardware Design” (PHI)
2. M. Abramovili, M.A. Breues, A. D. Friedman – “Digital Systems Testing and Testable Design” Jaico publications.

SYSTEM MODELLING & SIMULATION

(Common to VLSI and DECS)(Elective-III)

SUBJECT CODE: 13MVL1013

| L | P | C | INT | EXT |
|----------|----------|----------|------------|------------|
| 4 | 0 | 3 | 40 | 60 |

COURSE OBJECTIVES:

- The main objective of this course is to introduce basic concept of modeling and simulation of discrete events and systems.

COURSE OUTCOMES:

- Able to understand the concept of modeling, analysis and simulation of discrete events and systems.

UNIT – I

BASIC SIMULATION MODELING:

Systems, Models and Simulation, Discrete Event Simulation, Simulation of Single server queuing system, Simulation of Inventory System, Alternative approach to modeling and simulation.

UNIT – II

SIMULATION SOFTWARE:

Comparison of simulation packages with Programming Languages, Classification of Software, Desirable Software features, General purpose simulation packages – Arena, Extend and others, Object Oriented Simulation, Examples of application oriented simulation packages.

UNIT – III

BUILDING SIMULATION MODELS:

Guidelines for determining levels of model detail, Techniques for increasing model validity and credibility.

MODELING TIME DRIVEN SYSTEMS:

Modeling input signals, delays, System Integration, Linear Systems, Motion Control models, numerical experimentation.

UNIT – IV

EXOGENOUS SIGNALS AND EVENTS:

Disturbance signals, state machines, petri nets & analysis, System encapsulation.

MARKOV PROCESS:

Probabilistic systems, Discrete Time Markov processes, Random walks, Poisson processes, the exponential distribution, simulating a poison process, Continuous – Time Markov processes.

UNIT – V

EVEN DRIVEN MODELS:

Simulation diagrams, Queuing theory, simulating queuing systems, Types of Queues, Multiple Servers.

UNIT – VI

SYSTEM OPTIMIZATION:

System identification, Searches, Alpha/beta trackers, multidimensional optimization, modeling and simulation methodology.

TEXT BOOKS:

1. System Modeling & Simulation, An introduction – Frank L. Severance, John Wiley & Sons, 2001.
2. Simulation Modeling and Analysis – Averill M. Law, W. David Kelton, TMH, 3rd Edition, 2003.

REFERENCE BOOK:

1. Systems Simulation – Geoffrey Gordon, PHI, 1978.

MOS DEVICES MODELING

(Elective-III)

SUBJECT CODE: 13MVL1014

| L | P | C | INT | EXT |
|---|---|---|-----|-----|
| 4 | 0 | 3 | 40 | 60 |

COURSE OBJECTIVES:

- The main objective of this course is to introduce basic concept of modeling and simulation of MOS devices.

COURSE OUTCOMES:

- Able to understand the concept of modeling, analysis and simulation of MOS devices.

UNIT – I

OVERVIEW OF MOS:

Characteristics of a MOS transistor-Surface properties of Silicon : Energy band diagram for the ideal case-Calculation of the threshold voltage(v_t) – Non ideal effects-CV plots: importance – Ideal case – High frequency CV plots – low Frequency CV plots – Equations to CV plots – Deep depletion – Deviations from the Ideal CV plots - interface traps, Effect of AC signal on the interface states – Techniques to measure C_{it} , computation of C_s and P_s – Limitation in high frequency techniques – Comparison of measurements at high and low frequency techniques.

UNIT – II

Sources of oxide trapped charge – radiation created oxide trapped charge – Experimental results – How oxide Trapped charge can be annealed out – models to explain the technique – Shifts in threshold voltage in P-channel and N-channel MOSFET – Disadvantages – Shifts at dynamic bias – radiation hardening – Other alternatives dielectrics – gate metallization

UNIT – III

MOSFET- Parameters of importance – Qualitative analysis of MOSFET – Mathematical model of IV characteristics – SPICE level1, level2 , level3 models –

Change in velocity with electric field – Expression for I_d in the sub threshold region of operation.

UNIT – IV

Non uniform doping and effect on threshold voltage – short channel effect – Narrow width effect – Small geometry effects – Shrink and Scaling. Small signal analysis of MOSFET – Derivation of the different parameters associated with the small signal model – Cutoff frequency – Hot carrier effects – 1988 model – Monte Carlo analysis

UNIT – V

MOSFET DEVICES:

HMOS, DMOS, DIMOS, UMOS, VMOS, Sy MOSFET, SOS, Si MOX, BESOI, SEU, FAMOS, MCOS – Comparison with the conventional CMOS.

UNIT – VI

MOS DEVICE APPLICATIONS:

Depletion mode device – MOSFET connected as load devices - MOSFET as resistors, Static protection.

TEXT BOOK:

1. Dewitt G. Ong “Modern MOS technology: processes, Devices and Design”, Mcgraw Hill, 1984.

REFERENCE BOOKS:

1. Yannis Tsividis “Operation and Modeling of MOS Transistors”, Mcgraw Hill, 1999
2. Shoji.M “CMOS Digital circuit Technology”, Prentice Hall, 1988.
3. Sorab K.Ghandhi “Semiconductor device principle”, John wiley and sons, 1983.
4. Amar Mukerjee. “Introduction to Nmos and Cmos VLSI Systems design”, Prentice Hall, 1986

CPLD AND FPGA ARCHITECTURE AND APPLICATIONS

(Elective-IV)

SUBJECT CODE: 13MVL1015

| L | P | C | INT | EXT |
|----------|----------|----------|------------|------------|
| 4 | 0 | 3 | 40 | 60 |

COURSE OBJECTIVES:

- To have an overview of architectures & applications of CPLD and FPGA devices.
- To study the designing methods of CPLD and FPGA devices.

COURSE OUTCOMES:

At the end of the course, the student will be able to:

- Understand required building blocks to design CPLD and FPGA devices.
- Understand different CPLD and FPGA devices and basic programming skills.

UNIT –I

PROGRAMMABLE LOGIC DEVICES:

ROM, PLA, PAL, CPLD, FPGA – Features, Architectures, Programming, Applications and Implementation of MSI circuits using Programmable logic Devices.

UNIT – II

CPLDs: Complex Programmable Logic Devices, Altera series – Max 5000/7000 series and Altera FLEX logic-10000 series CPLD, AMD's- CPLD (Mach 1 to 5), Cypress FLASH 370 Device technology, Lattice pLSI's architectures – 3000 series – Speed performance and in system programmability.

UNIT – III

FPGAs: Field Programmable Gate Arrays- Logic blocks, routing architecture, design flow, technology mapping for FPGAs, Case studies Xilinx XC4000 & ALTERA's FLEX 8000/10000, FPGAs: AT &T ORCA's

UNIT – IV

FINITE STATE MACHINES (FSM):

Top Down Design, State Transition Table, State assignments for FPGAs, Realization of state machine charts using PAL, Alternative realization for state machine charts using microprogramming, linked state machine, encoded state machine.

FSM ARCHITECTURES:

Architectures Centered around non registered PLDs, Design of state machines centered around shift registers, One_Hot state machine, Petrinets for state machines- Basic concepts and properties, Finite State Machine-Case study.

UNIT – V

DESIGN METHODS:

One –hot design method, Use of ASMs in one-hot design method, Applications of onehot design method, Extended Petri-nets for parallel controllers, Meta Stability, Synchronization, Complex design using shift registers.

UNIT – VI

SYSTEM LEVEL DESIGN:

Controller, data path designing, Functional partition, Digital front end digital design tools for FPGAs & ASICs, System level design using mentor graphics EDA tool (FPGA Advantage), Design flow using CPLDs and FPGAs.

CASE STUDIES:

Design considerations using CPLDs and FPGAs of parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - S. Trimberger, Edr, 1994, Kluwer Academic Publications.
2. Engineering Digital Design - RICHARD F.TINDER, 2nd Edition, Academic press.
3. Fundamentals of logic design-Charles H. Roth, 4th Edition Jaico Publishing House.

REFERENCES BOOKS:

1. Digital Design Using Field Programmable Gate Array, P.K.Chan & S. Mourad, 1994, Prentice Hall.
2. Field programmable gate array, S. Brown, R.J.Francis, J.Rose ,Z.G.Vranesic, 2007, BSP.

NETWORK SECURITY AND CRYPTOGRAPHY

(Common to VLSI and DECS)(Elective-IV)

SUBJECT CODE: 13MVL1016

| L | P | C | INT | EXT |
|---|---|---|-----|-----|
| 4 | 0 | 3 | 40 | 60 |

COURSE OBJECTIVES:

- Learn fundamentals of cryptography and its application to network security.
- Understand network security threats, security services, and countermeasures.
- Acquire background on well known network security protocols.
- Understand vulnerability analysis of network security.

COURSE OUTCOMES:

- Understand network security and cryptography concepts and applications.
- The student can able to apply security principles to system design.
- Identify and investigate network security threats.
- Analyze and design network security protocols.

UNIT – I

SYMMETRIC CIPHERS:

Overview – classical Encryption Techniques, Block Ciphers and the Data Encryption standard, Introduction to Finite Fields, Advanced Encryption standard, Contemporary Symmetric Ciphers, Confidentiality using Symmetric Encryption.

PUBLIC-KEY ENCRYPTION AND HASH FUNCTIONS:

Introduction to Number Theory, Public-Key Cryptography and RSA, Key Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication and Hash Functions, Hash Algorithms, Digital Signatures and Authentication Protocols.

UNIT – II

NETWORK SECURITY PRACTICE:

Authentication Applications, Kerbors, X.509 Authentication Service, Electronic mail Security, Pretty Good Privacy, S/MIME, IP Security architecture, Authentication Header, Encapsulating Security Payload, Key Management.

UNIT – III

SYSTEM SECURITY:

Intruders, Intrusion Detection, Password Management, Malicious Software, Firewalls, Firewall Design Principles, Trusted Systems.

WIRELESS SECURITY:

Introduction to Wireless LAN Security Standards, Wireless LAN Security Factors and Issues.

UNIT – IV

ENCRYPTION TECHNIQUES:

Conventional techniques, Modern techniques, DES, DES chaining, Triple DES, RSA algorithm, Key management, Message Authentication, Hash Algorithm, Authentication requirements, functions secure Hash Algorithm, Message digest algorithm, digital signatures, AES Algorithms.

UNIT – V

SECURE NETWORKING THREATS:

Attack Process, Attacker Types. Vulnerability Types, Attack Results, Attack Taxonomy, Threats to Security, Physical security, Biometric systems, monitoring controls, Data security, intrusion, detection systems.

UNIT – VI

DESIGNING SECURE NETWORKS:

Components of a Hardening Strategy, Network Devices, Host Operating Systems, Applications, Based Network Services, Rogue Device Detection, Network Security Technologies, the Difficulties of Secure Networking, Security Technologies,

Emerging Security Technologies General Design Considerations, Layer 2 Security Considerations, IP Addressing Design Considerations - ICMP Design Considerations, Routing Considerations, Transport Protocol Design Considerations.

TEXT BOOKS:

1. William Stallings, “Cryptography and Network Security – Principles And Practices”, Pearson Education, 3rd Edition, 2003.
2. Sean Convery, “ Network Security Architectures, Published by Cisco Press, First Ed. 2004.

REFERENCE BOOKS:

1. Atul Kahate, “Cryptography and Network Security”, Tata McGraw Hill, 2003.
2. Bruce Schneier, “Applied Cryptography”, John Wiley and Sons Inc, 2001.
3. Stewart S. Miller, “Wi-Fi Security”, McGraw Hill, 2003.
4. Charles B. Pfleeger, Shari Lawrence Pfleeger, “Security In Computing”, 3rd Edition, Pearson Education, 2003.
5. Jeff Crume, “Inside Internet Security” Addison Wesley, 2005.

MIXED SIGNAL SIMULATION LABORATORY

SUBJECT CODE: 13MVL1102

| L | P | C | INT | EXT |
|---|---|---|-----|-----|
| 0 | 4 | 2 | 40 | 60 |

COURSE OBJECTIVES:

- Students will learn industrial techniques for mixed-signal IC test, which include dc measurement, frequency response, harmonic and intermodulation distortion, and noise behavior.
- Students will apply these techniques to analog, sampled-data mixed-signal, RF, and high-speed digital channels.

COURSE OUTCOMES:

- The student can able to design mixed signal circuits using VLSI CAD tools.
- The student can understand mixed signal design flow.

By considering suitable complexity Mixed-Signal application based circuits (circuits consisting of both analog and digital parts), the students are required to perform the following aspects using necessary software tools:

1. Analog Circuits Simulation using Spice Software.
2. Digital Circuits Simulation using Xilinx Software.
3. Mixed Signal Simulation Using Mixed Signal Simulators.
4. Layout Extraction for Analog & Mixed Signal Circuits.
5. Parasitic Values Estimation from Layout.
6. Layout Vs Schematic.
7. □ Net List Extraction.
8. Design Rule Checks.