ACADEMIC REGULATIONS
COURSE STRUCTURE AND SYLLABI
FOR

M.TECH

Digital Electronics and Communication Systems

(Department of Electronics and Communication Engineering)

From The Academic Year 2013-2014

ADITYA Institute of Technology And Management

(AUTONOMOUS)

Approved by AICTE, Permanently Affiliated to JNTUK, Kakinada

Accredited by NBA & NAAC, Recognised by UGC under 2(f) & 12(b)

K Kotturu, TEKKALI, Srikakulam Dist., A.P

VISION

To evolve into a premier engineering institute in the country by continuously enhancing the range of our competencies, expanding the gamut of our activities and extending the frontiers of our operations.

MISSION

Synergizing knowledge, technology and human resource, we impart the best quality education in Technology and Management. In the process, we make education more objective so that the efficiency for employability increases on a continued basis.

Academic Regulations 2013 for M.Tech (Regular)

(With effect from batch admitted in the academic year 2013-2014)

The M.Tech Degree of the Aditya Institute of Technology and Management (Autonomous), Tekkali shall be conferred on candidates who are admitted to the programme and fulfill all the requirements for the award of the Degree.

1. ELIGIBILITY FOR ADMISSIONS:

Admission to the above programme shall be made subject to the eligibility, qualifications and specialization prescribed by the University from time to time. Admissions shall be made on the basis of merit rank obtained by the qualifying candidate in GATE / PGCET, subject to reservations prescribed by the Govt. of AP from time to time.

2. AWARD OF M. Tech DEGREE:

2.1 A student shall be declared eligible for award of the M.Tech degree, if he/she pursues a course of study and completes it successfully in not less than two academic years and not more than four consecutive academic years and registered for **80** credits and secure **80** credits.

2.2 A student, who fails to fulfill all the academic requirements for the award of the degree within four academic years from the year of his/her admission, shall forfeit his/her seat in M.Tech course.

2.3 The minimum clear instruction days for each semester are 95.

3. ATTENDANCE:

3.1 A candidate shall be deemed to have eligibility to write End Semester examinations if he/she has put in a minimum of 75% of attendance in aggregate of all the subjects.

3.2 Condonation of shortage of attendance up to 10% (65% and above, and below 75%) may be given by the College academic committee.

3.3 Condonation of shortage of attendance shall be granted only on genuine and valid reasons on representations by the candidate with supporting evidence.

3.4 Shortage of attendance below 65% shall in NO case be condoned.

3.5 A candidate shall not be promoted to the next semester unless he/she fulfills the attendance requirements of the present semester.

3.6 A stipulated fee shall be payable towards condonation of shortage of attendance.

4. COURSE OF STUDY:

The following specializations are offered at present for the M.Tech course of study.

1	Digital Electronics and Communication Systems
2	VLSI System Design
3	Power Electronics and Electric Drives
4	Computer Science and Engineering
5	Information Technology
6	Thermal Engineering

5. EVALUATION:

The performance of the candidate in each semester shall be evaluated subject-wise, with a Maximum of 100 marks for theory and100 marks for Laboratory, on the basis of Internal Evaluation and End Semester Examination.

5.1 For the theory subjects 60 marks shall be awarded based on the performance in the End Semester Examination. Out of 40 internal marks 30 marks are assigned for subjective exam, 5 marks for subjective assignments and 5 marks for seminars. The internal evaluation for 30 marks shall be made based on the **average** of the marks secured in the two Mid Term-Examinations conducted, one in the middle of the Semester and the other immediately after the completion of instruction. Each midterm examination shall be conducted in a duration of 120 minutes and question paper shall contain **4** questions. The student should answer all **4** questions.

5.2 For practical subjects, 60 marks shall be awarded based on the performance in the End Semester Examinations. Out of 40 internal marks 20 marks are assigned based on day to day evaluation and 20 marks are assigned based on the internal test.

5.3 There shall be a technical seminar presentation during 3rd semester. For technical seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the Department in a report form and shall make an oral presentation before the Departmental Committee. The Departmental Committee consists of Head of the Department, supervisor and two other senior faculty members of the department. For technical seminar there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% to be declared successful.

5.4 A candidate shall be deemed to have secured the academic requirement in a subject if he/she secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

5.5 In case the candidate does not secure the minimum academic requirement in any Subject (as specified in 5.4) he has to reappear for the supplementary Examination in that subject.

5.6 The viva-voce examination shall be conducted at the end of the course work and after the candidate passing all subjects.

5.7 Laboratory examination for M.Tech courses must be conducted with two Examiners, one of them being Laboratory Class Teacher and second examiner shall be external examiner.

6. EVALUATION OF PROJECT/DISSERTATION WORK:

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the Project Review Committee.

6.1 A Project Review Committee (PRC) shall be constituted with Principal as chair person, Head of the department, one senior faculty member and project guide.

6.2 Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects (theory and practical).

6.3 After satisfying 6.2, a candidate has to submit, in consultation with his / her project supervisor, the title, objective and plan of action of his project work (Based on a publication in a Peer Reviewed Journal) to the Project Review Committee for its approval before the second semester end examinations. After obtaining the approval of the Committee, the student can initiate the Project work after the second semester end examinations.

6.4 Every candidate shall work on projects approved by the PRC of the college.

6.5 If a candidate wishes to change his supervisor or topic of the project, he/she can do so with approval of the PRC. However, the Project Review Committee (PRC) shall examine whether the change of topic/supervisor leads to a major change of his initial plans of project proposal. If so, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

6.6 A candidate shall submit status report in two stages at least with a gap of 3 months between them.

6.7 The work on the project shall be initiated in the beginning of the second year/III semester and minimum duration of the project is two semesters. The candidate shall identify the problem, Literature survey, design/modeling part of the problem i.e. almost 35% of his dissertation/project work should complete in the III semester itself and it will be evaluated by PRC. If the candidate fails to get the satisfactory report, he has to re-register for the project/dissertation work.

6.8 A candidate shall be allowed to submit the project report only after fulfilling the attendance requirements of all the semesters with approval of PRC and not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Principal (through Head of the Department) and shall make an oral presentation before the PRC.

6.9 The Candidate may be permitted to submit the Project Report, if only after the work is Published/Accepted to be Published in a Journal / International conference of repute and relevance.

6.10 Three copies of the Project Thesis certified by the supervisor shall be submitted to the College/Institute.

6.11 The thesis shall be adjudicated by external examiner from outside the college.

6.12 The viva-voce examination shall be conducted by a board consisting of the supervisor, Head of the Department and the examiner outside the college who adjudicated the Thesis.

6.13 The student has to clear all the subjects of M.Tech course before submission of the project thesis/ dissertation

The Board shall jointly report candidates work as :

A. Excellent

B. Good

C. Satisfactory

D. Unsatisfactory

Head of the Department shall coordinate and make arrangements for the conduct of viva-voce examination. If the report of the viva-voce is unsatisfactory, the candidate has to retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second viva-voce examination, the candidate may be asked to submit a new project proposal to PRC starting with 6.5

7. METHOD OF AWARDING LETTER GRADES AND GRADE POINTS FOR A COURSE.

A letter grade and grade points will be awarded to a student in each course based on his/her performance as per the grading system given below.

Table: Grading System for M.Tech. Programme

Percentage of Marks	Grade Points	Letter Grade
90-100	10	S
80-89	9	A
70-79	8	B
60-69	7	C
50-59	6	D
40-49	5	E
< 40	0	F (Fail)

7.1 Calculation of Semester Grade Points Average (SGPA)* for semester

The performance of each student at the end of the each semester is indicated in terms of SGPA. The SGPA is calculated as below:

$$SGPA = \frac{\Sigma(CR \times GP)}{\Sigma CR}$$ (for all courses passed in semester)

Where CR = Credits of a Course

GP = Grade points awarded for a course

*SGPA is calculated for the candidates who passed all the courses in that semester.

7.1.1 Calculation of Cumulative Grade Points Average (CGPA) and Award of Division for Entire Programme.

The CGPA is calculated as below:

$$CGPA = \frac{\Sigma(CR \times GP)}{\Sigma CR}$$ (for entire programme)

Where CR = Credits of a course

GP = Grade points awarded for a course

Table: Award of Divisions

CGPA	DIVISION
≥ 8	First Class with distinction
≥ 7 - < 8	First Class
≥ 6 - < 7	Second Class
< 6	Fail

After a student has satisfied the requirements prescribed for the completion of the programme and is eligible for receiving the award of M.Tech. Degree, he shall be placed in one of the above three divisions.

8. WITH-HOLDING OF RESULTS:

If the candidate has not paid any dues to the college or if any case of indiscipline is pending against him / her, the result of the candidate will be withheld and he/she will not be allowed into the next higher semester. The issue of the degree is liable to be with held in such cases.

9. TRANSITORY REGULATIONS:

Candidate who have discontinued or have been detained for want of attendance or who have failed after having undergone the course are eligible for admission to the same or equivalent subjects as and when subjects are offered, subject to 5.5 and 2.0

10. GENERAL:

10.1 The academic regulations should be read as a whole for purpose of any Interpretation.

10.2 In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Principal is final.

10.3 The Institute may change or amend the academic regulations and syllabus at any time and the changes and amendments made shall be applicable to all the students with effect from the date notified by the college.

10.4 Wherever the word he, him or his occur, it will also include she, her and hers.

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M.TECH COURSE STRUCTURE

M. Tech. (DECS) – 1st SEMESTER							
S. No.	**Sub. Code**	**SUBJECT**	**L**	**P**	**C**	**INT**	**EXT**
1	13MVL1001	Digital System Design	4	-	3	40	60
2	13MVL1002	VLSI Technology & Design	4	-	3	40	60
3	13MVL1003	Analog & Digital IC Design	4	-	3	40	60
4	13MDE1001	Detection and estimation of signals	4	-	3	40	60
5	**Elective – I**		4	-	3	40	60
	13MVL1005	Digital Data Communications					
	13MVL1006	Embedded & Real Time Systems					
6	**Elective – II**		4	-	3	40	60
	13MDE1002	Advanced Digital Signal Processing					
	13MDE1003	Transforms & Probability Theory					
7	13MVL1101	HDL Programming Laboratory	-	4	2	40	60
TOTAL			**28**		**20**	**700**	

M. Tech. (DECS) – 2nd SEMESTER							
S. No.	**Sub. Code**	**SUBJECT**	**L**	**P**	**C**	**INT**	**EXT**
1	13MVL1009	DSP Processors and architecture	4	-	3	40	60
2	13MDE1004	Wireless Communication & Networks	4	-	3	40	60
3	13MDE1005	Optical Communication	4	-	3	40	60
4	13MDE1006	Coding Theory & Practice	4	-	3	40	60
5	**Elective – III**		4	-	3	40	60
	13MVL1013	System Modeling & Simulation					
	13MDE1007	Radar Signal Processing					
6	**Elective – IV**		4	-	3	40	60
	13MDE1008	Image and Video Processing					
	13MVL1016	Network Security and Cryptography					
7	13MDE1101	Digital Signal, Image and Video processing Lab	-	4	2	40	60
TOTAL			**28**		**20**	**700**	

M. Tech. (DECS) – 3rd SEMESTER							
S. No.	**Sub. Code**	**SUBJECT**	**L**	**P**	**C**	**INT**	**EXT**
1	13MDE2201	Technical Seminar	-	-	2	100	-
2	13MDE2202	Project Work Phase-1	-	-	18	-	-
TOTAL			**-**		**20**	**100**	

M. Tech. (DECS) – 4th SEMESTER							
S. No.	**Sub. Code**	**SUBJECT**	**L**	**P**	**C**	**INT**	**EXT**
1	13MDE2203	Project Work Phase-2	-	-	20	-	-
TOTAL			**-**		**20**	**-**	

L – Lecture hours/Week; P – Practical hours/ Week; C – Credits; INT – Internal Marks; EXT – External Marks;

DIGITAL SYSTEM DESIGN

(Common to VLSI and DECS)

SUBJECT CODE: 13MVL1001

L	P	C	INT	EXT
4	0	3	40	60

COURSE OBJECTIVES:

- The main objective of this course is to introduce concepts and designing principles of various digital systems used in designing of digital circuits.

COURSE OUTCOMES:

- Able to understand the concept and designing of various digital systems. Acquire knowledge in the testing of designed digital systems.

UNIT – I

DESIGN OF DIGITAL SYSTEMS:

ASM charts, Hardware description language and control sequence method, Reduction of state tables, State assignments.

UNIT – II

SEQUENTIAL CIRCUIT DESIGN:

Design of Iterative circuits, Design of sequential circuits using ROMs and PLAs, Sequential circuit design using CPLD, FPGAs.

UNIT – III

FAULT MODELING:

Fault classes and models – Stuck at faults, bridging faults, transition and intermittent faults.

FAULT DIAGNOSIS IN SEQUENTIAL CIRCUITS:

State identification and fault detection experiment. Machine identification, Design of fault detection experiment.

UNIT – IV

TEST GENERATION:

Fault diagnosis of Combinational circuits by conventional methods – Path Sensitization technique, Boolean difference method, Kohavi algorithm.

TEST PATTERN GENERATION:

D – algorithm, PODEM, Random testing, transition count testing, Signature analysis and testing for bridging faults.

UNIT – V

PROGRAMMING LOGIC ARRAYS:

Design using PLA's, PLA minimization and PLAfolding.

PLA TESTING:

Fault models, Test generation and Testable PLA design.

UNIT – VI

ASYNCHRONOUS SEQUENTIAL MACHINE:

Fundamental mode model, flow table, state reduction, minimal closed covers, races, cycles and hazards.

TEXT BOOKS:

1. Z. Kohavi – "Switching & finite Automata Theory" (TMH).

2. N. N. Biswas – "Logic Design Theory" (PHI).

3. Nolman Balabanian, Bradley Calson – "Digital Logic Design Principles" – Wily Student Edition 2004.

REFRENCE BOOKS:

1. M. Abramovici, M. A. Breues, A. D. Friedman – "Digital System Testing and Testable Design", Jaico Publications.

2. Charles H. Roth Jr. – "Fundamentals of Logic Design".

3. Frederick. J. Hill & Peterson – "Computer Aided Logic Design" – Wiley 4th Edition.

VLSI TECHNOLOGY & DESIGN

(Common to VLSI and DECS)

SUBJECT CODE: 13MVL1002

L	P	C	INT	EXT
4	0	3	40	60

COURSE OBJECTIVES:

- The main objective of this course is to introduce basic concepts of microelectronics, layout designing, floor planning and algorithms used in the chip designing process.

COURSE OUTCOMES:

- Student is able to understand the concepts of and electrical properties of MOS technologies.
- Student is able to understand different types layout designing tools and floor planning methods used in chip design.
- Student is able to design combinational logic networks and sequential systems.
- Student is able to understand CAD algorithms used in chip design.

UNIT – I

REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES: (MOS, CMOS, Bi CMOS)

Technology trends and projections. Lithography, Oxidation, Ion implantation, Metalization and Diffusion techniches.

BASIC ELECTRICAL PROPERTIES OF MOS, CMOS & BICOMS CIRCUITS:

Ids-Vds relationships, Threshold voltage Vt, Gm, Gds and Wo, Pass Transistor, MOS,CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT – II

LAYOUT DESIGN AND TOOLS:

Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

LOGIC GATES & LAYOUTS:

Static complementary gates, switch logic, Alternative gate circuits, low power gates, Resistive and Inductive interconnect delays.

UNIT – III

COMBINATIONAL LOGIC NETWORKS:

Layouts, Simulation, Network delay, interconnect design, power optimization, Switch logic networks, Gate and Network testing.

UNIT – IV

SEQUENTIAL SYSTEMS:

Memory cells and Arrays, clocking disciplines, System Design, power optimization, Design validation and testing.

UNIT – V

FLOOR PLANNING & ARCHITECTURE DESIGN:

Floor planning methods, off-chip connections, High-level synthesis, Architecture for low power, SOCs and Embedded CPUs, Architecture testing.

UNIT – VI

INTRODUCTION TO CAD SYSTEMS (ALGORITHMS) AND CHIP DESIGN:

Layout Synthesis and Analysis, Scheduling and printing, Hardware/Software Co-design, chip design methodologies- A simple Design example.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian et. al (3 authors) PHI of India Ltd.,2005.

2. Modern VLSI Design, 3rd Edition, Wayne Wolf, Pearson Education, 5th Indian Reprint, 2005.

REFERENCE BOOKS:

1. Principals of CMOS Design – N.H.E Weste, K.Eshraghian, Adison Wesley, 2nd Edition.
2. Introduction to VLSI Design – Fabricius, MGH International Edition, 1990.
3. CMOS Circuit Design, Layout and Simulation – Baker, Li Boyce, PHI, 2004.
4. VLSI Technology - 2nd Edn..- S.M.Sze.

ANALOG AND DIGITAL IC DESIGN

(Common to VLSI and DECS)

SUBJECT CODE: 13MVL1003

L	P	C	INT	EXT
4	0	3	40	60

COURSE OBJECTIVES:

- The course provides understanding the main principles of various analog and digital building blocks used in IC design.

COURSE OUTCOMES:

- Able to understand the concepts analog building blocks like operational amplifier, phase locked loops and switched capacitors.
- Able to understand the concepts and designing of digital building blocks like combinational logic circuits, sequential logic circuits using VHDL.

UNIT – I

OPERATIONAL AMPLIFIERS:

General considerations one – state op-amps, two stage op-amps-gains boosting stage- comparison I/P range limitations slew rate.

CURRENT MIRRORS AND SINGLE STAGE AMPLIFIERS:

simple COMS, BJT current mirror, Cascode Wilson Wilder current mirrors. Common Source amplifier source follower, common gate amplifier

NOISE: Types of Noise – Thermal Noise-flicker noise- Noise in opamps- Noise in common source stage noise band width.

UNIT – II

PHASED LOCKED LOOP DESIGN:

PLL concepts- The phase locked loop in the locked condition Integrated circuit PLLs – phase Detector- Voltage controlled oscillator case study: Analysis of the 560 B Monolithic PLL.

UNIT – III

SWITHCHED CAPACITORS CIRCUITS:

Basic Building blocks op-amps capacitors switches – non-over lapping clocks-Basic operations and analysis-resistor equivalence of la switched capacitor-parasitic sensitive integrator parasitic insensitive integrators signal flow graph analysis-First order filters- switch sharing fully differential filters – charged injections-switched capacitor gain circuits parallel resistor –capacitor circuit – preset table gain circuit – other switched capacitor circuits – full wave rectifier – peak detector sinusoidal oscillator.

UNIT – IV

LOGIC FAMILIES & CHARACTURISTICS:

COMS, TTL, ECL, logic families COMS/ TTL, interfacing comparison of logic families.

COMBINATIONAL LOGIC DESIGN USING VHDL:

VHDL modeling for decoders, encoders, multiplexers, comparison, adders and subtractors.

SEQUENCIAL IC DESIGN USING VHDL:

VHDL modeling for larches, flip flaps, counters, shift registers FSMs. ASM charts.

UNIT – V

DIGITAL INTEGRADED SYSTEM BUILDING BLOCKS:

Multiplexers and decoders – barrel shifters counters digital single bit adder.

MEMORIES:

ROM Internal structure, 2D decoding commercial type timing and applications, RAM internal structure.

CPLD:

XC 9500 series family CPLD architecture – CLB internal architecture, I/O block internal structure.

FPGA:

Conceptual of view of FPGA – classification based on CLB internal architecture I/O block architecture.

UNIT – VI

COMPARATORS:

Using an op-amp for a comparator-charge injection errors- latched comparator.

NYQUIST RATE D/A CONVERTERS:

Decoder based converter resistor storing converters folded resister string converter – Binary scale converters – Binary weighted resistor converters – Reduced resistance ratio ladders – R-2R based converters – Thermometer code current mode D/A converters.

NYQUIST RATE A/D CONVERTERS:

Integrating converters – successive approximation converters. DAC based successive approximation – flash converters time interleaved A/D converters.

TEXT BOOKS:

1. Analog Integrated circuit Design by David A Johns, Ken Martin, John Wiley & Sons.
2. Analysis and design of Analog Integrated Circuits, by Gray, Hurst Lewis, Meyer. John Wiley & Sons.
3. Design of Analog CMOS Integrated Circuits, Behzad Razavi, TMH
4. Digital Integrated Circuit Design by Ken Martin, Oxford University 2000
5. Digital Design Principles & Practices" by John F Wakerly, Pearson Education & Xilinx Design Series, 3rd Ed.(2002)

REFERENCE BOOKS:

1. Ken Martin, Digital Integrated Circuit Design Oxford University,2000.
2. John F Wakerly, "Digital Design Principles & Practices", Pearson Education & Xilinx Design Series, 3rd Ed.(2002)

3. Samir Palnitkar, “Verylog HDL-A Guide to Digital Design and Synthesis”, Prentice Hall India, (2002)
4. Douglas J Smith, “HDL Chip Design, a practical Guide for Designing, Synthesizing and simulating ASICs and FPGAs

DETECTION AND ESTIMATION OF SIGNALS

SUBJECT CODE: 13MDE1001

L	P	C	INT	EXT
4	0	3	40	60

COURSE OBJECTIVES:

- To cover the theoretical foundations of detection and estimation theory and its applications in digital communication, sensing, imaging and radar systems.

COURSE OUTCOMES:

- Able to understand the concepts of discrete time signals, random signals, detection and estimation of signals in noise environment.

UNIT – I

INTRODUCTION TO DISCRETE-TIME SIGNALS:

Fourier series representation and Fourier Transform of a discrete time signal. Examples: Amplitude and phase spectrum. Frequency content and sampling rates, Transfer function, Frequency response, problems.

UNIT – II

RANDOM DISCRETE-TIME SIGNALS:

Review of probability – Random data: moments and histograms – Generation and shaping of pseudorandom noise. Filtered random signals – Autocorrelation and power spectral density – Sampling band limited random signals.

UNIT – III

OPTIMUM ALGORITHMS FOR DETECTION OF SIGNALS IN NOISE – 1:

Minimum probability of Error. Criterion, Neyman – Person criterion for Radar, Applications to Air Traffic Control radar, detection of constant and variable – amplitude signals.

UNIT – IV

OPTIMUM ALGORITHMS FOR DETECTION OF SIGNALS IN NOISE – 2:

Matched filters. Optimum formulation, detection of Random signals – Simple problems there on with multisampling cases.

UNIT – V

ESTIMATION OF SIGNALS IN NOISE:

Linear mean squared estimation – Bayes estimator, its examples – Maximum likelihood estimate of parameters of linear system.

UNIT – VI

RECURSIVE LINEAR MEAN SQUARED ESTIMATION:

Estimation of a signal parameter. Estimation of time-varying signals – Kalman filtering – Filtering signals in noise – Treatment restricted to two variable case only – Simple problems, Application to Air Traffic Control radar tracking.

TEXT BOOK:

1. Signal processing: Discrete Spectral analysis, Detection and Estimation, Mischa Schwartz and Leonard Shaw, Mc-Graw Hill Book Company, 1975.

REFERENCE BOOKS:

1. E.L. Van Trees, Detection, Estimation and Modulation Theory, Wiley, New York, 1968.

2. Shanmugam and Breipohl, 'Detection of signals in noise and estimation', John Wiley & Sons, New York, 1985.

3. Srinath, Rajasekaran & Viswanathan, Introduction to statistical Signal processing with Applications, Prentice Hall of India, New Delhi, 110 001,1989.

DIGITAL DATA COMMUNICATIONS

(Common to VLSI and DECS)(Elective-I)

SUBJECT CODE: 13MVL1005

L	P	C	INT	EXT
4	0	3	40	60

COURSE OBJECTIVES:

- The main objective of this course is to introduce basic concepts of various methods used in transmitting digital data using wired and wireless communication.

COURSE OUTCOMES:

- Student is able to understand different types of digital modulation techniques.
- Student is able to understand the concepts of digital multiplexing, local area networks and multimedia.
- Student is able to understand various interfaces and methods used to transmit digital data.

UNIT – I

DIGITAL MODULATION TECHNIQUES:

FSK, MSK, BPSK, QPSK, 8-PSK, 16-PSK, 8- QAM, 16 - QAM, Band width efficiency carrier recovery DPSK, clock recovery, Probability of error and bit error rate.

UNIT – II

DATA COMMUNICATIONS:

Serial, Parallel configuration, Topology, Transmission modes, codes, Error Control Synchronization, LCU.

UNIT – III

Serial and Parallel Interfaces, Telephone Networks and Circuits and data modems.

Data Communication Protocols, Character and block Mode, Asynchronous and Synchronous Protocols, public Data Networks, ISDN.

UNIT – IV

DIGITAL MULTIPLEXING:

TDM, T1 carrier, CCITT, CODECS, COMBO CHIPS, North American Hierarchy, Line Encoding, T-carrier, Frame Synchronization Inter Leaving Statistical TDM FDM , Hierarchy ,Wave Division Multiplexing .

UNIT – V

LOCAL AREA NETWORKS:

token ring, Ethernet, Traditional, Fast and GIGA bit Ethernet, FDDI.

WIRELESS LANS IEEE 802.11:

Architecture Layers, Addressing, Blue Tooth Architecture Layers, l2 Cap, Other Upper Layers.

UNIT – VI

MULTI MEDIA:

Digitalizing Video and Audio Compression Streaming Stored and Live Video and Audio, Real Time Interactive Video and Audio, VOIP.

TEXT BOOKS:

1. Electronic communication systems, fundamentals through advanced - W. TOMASI, Pearson 4th Edition.
2. Data communication and networking - B.A. Forouzen

EMBEDDED AND REAL TIME SYSTEMS

(Common to VLSI and DECS)(Elective-I)

SUBJECT CODE: 13MVL1006

L	P	C	INT	EXT
4	0	3	40	60

COURSE OBJECTIVES:

- To introduce the basic concepts of embedded systems.

To clearly differentiate the different issues that arises in designing soft and hard real-time systems.

- To explain the various concepts of time that arises in real-time systems.

COURSE OUTCOMES:

- The student got familiarity with design of embedded systems.
- Master the core knowledge of real-time embedded system design.
- Develop skills for application of core knowledge.

UNIT – I

INTRODUCTION:

Embedded systems over view, design challenges, processor technology, Design technology, Trade-offs. Single purpose processors RT-level combinational logic, sequential logic(RTlevel), custom purpose processor design(RT -level), optimizing custom single purpose processors.

GENERAL PURPOSE PROCESSORS:

Basic architecture, operations, programmer's view, development environment, Application specific Instruction –Set processors (ASIPs)-Micro controllers and Digital signal processsors.

UNIT – II

STATE MACHINE AND CONCURRENT PROCESS MODELS:

Introduction, models Vs Languages, finite state machines with data path model(FSMD),using state machines, program state machine model(PSM,

concurrent process model, concurrent processes, communication among processes, synchronization among processes, Implementation, data flow model, real-time systems.

UNIT – III

COMMUNICATION PROCESSES:

Need for communication interfaces, RS232/UART, RS422/RS485,USB, Infrared, IEEE1394 Firewire, Ethernet, IEEE 802.11, Blue tooth.

UNIT – IV

EMBEDDED/RTOS CONCEPTS-I:

Architecture of the Kernel, Tasks and task scheduler, interrupt service routines, Semaphores, Mutex.

EMBEDDED/RTOS CONCEPTS -II:

Mailboxes, Message Queues, Event Registers, Pipes-Signals.

UNIT – V

EMBEDDED/RTOS CONCEPTS – III:

Timers-Memory Management-Priority inversion problem embedded operating systems-Embedded Linux-Real-time operating systems-RT Linux-Handheld operating systems-Windows CE.

UNIT – VI

DESIGN TECHNOLOGY:

Introduction, Automation, Synthesis, parallel evolution of compilation and synthesis, Logic synthesis, RT synthesis, Behavioral Synthesis, Systems Synthesis and Hardware/Software Co-Design, Verification, Hardware/Software co-simulation, Reuse of intellectual property codes.

TEXT BOOKS:

1. Embedded System Design-A Unified Hardware/Software Introduction- Frank Vahid, Tony D. Givargis, John Wiley & Sons, Inc.2002.

2. Embedded/Real Time Systems- KVKK prased, Dreamtech press-2005.

3. Introduction to Embedded Systems - Raj Kamal, TMS-2002.

REFERENCE BOOKS:

1. Embedded Microcomputer Systems-Jonathan W.Valvano, Books/Cole,Thomson Leaarning.

2. An Embedded Software Primer- David E.Simon, pearson Ed.2000

ADVANCED DIGITAL SIGNAL PROCESSING

(Elective-II)

SUBJECT CODE: 13MDE1002

L	P	C	INT	EXT
4	0	3	40	60

COURSE OBJECTIVES:

- To have an overview of signals and systems and DFT & FFT Transforms.
- To study the design of IIR & FIR filters.
- To study the structures and analysis of DSP processors.

COURSE OUTCOMES:

At the end of the course, the student will be able to:

- Understand types of digital signals and Transforms and its application to signals and systems.
- Design of IIR & FIR filters. Understand different DSP processors and basic programming skills.

UNIT – I

DISCRETE FOURIER TRANSFORMS:

Properties of DFT, Linear Filtering methods based on the DFT, Overlap-save, Overlap -Add methods, frequency analysis of signals. Radix-2 FFT and Split-Radix FFT algorithms The Goertzel and Chirp Z transform algorithms.

UNIT – II

DESIGN OF IIR FILTERS:

Design of IIR filters using Butterworth & Chebyshev approximations, frequency transformation techniques, structures for IIR systems –cascade, parallel, lattice & lattice-ladder structures.

UNIT – III

DESIGN OF FIR FILTERS:

Fourier series method, Windowing techniques, design of digital filters based on least – squares method, pade approximations, least squares design, wiener filter methods.

UNIT – IV

STRUCTURES FOR FIR SYSTEMS:

cascade, parallel, lattice & lattice-ladder structures.

UNIT – V

POWER SPECTRAL ESTIMATION:

Estimation of spectra from finite duration observation of signals, Non-parametric methods: Bartlett,Welch & Blackmann & Tukey methods. Relation between auto correlation & model parameters, Yule-Waker & Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT – VI

ANALYSIS OF FINITE WORD LENGTH EFFECTS IN FIXED-POINT DSP SYSTEMS:

Fixed, Floating Point Arhimetic – ADC quantization noise & signal quality – Finite wordlength effect in IIR digital Filters – Finite word-length effects in FFT algorithms.

TEXTBOOKS:

1. Digital Signal Processing –Principles, Algorithms Applications by J.G.Proakis & D.G.Manolokis, PHI.

2. Discrete Time signal processing - Alan V Oppenheim & Ronald W Schaffer, PHI.

3. DSP – A Pratical Approach – Emmanuel C.Ifeacher Barrie. W. Jervis, Pearson Education.

REFERENCE BOOK:

1. Modern spectral Estimation techniques by S. M .Kay, PHI, 1997

TRANSFORMS & PROBABILITY THEORY

(Elective-II)

SUBJECT CODE: 13MDE1003

L	P	C	INT	EXT
4	0	3	40	60

COURSE OBJECTIVES:

- To have an overview of 1D & 2D transfoms and wavelet transforms.
- To study the concepts of random variables and random process.

COURSE OUTCOMES:

At the end of the course, the student will be able to:

- Understand types of 1D & 2D transforms and their applications.
- Understand the importance of wavelet transform and its applications.
- Understand different DSP processors and basic programming skills.
- Acquired the fundamental concepts of probability theory.
- Learn some important results on probability.
- Acquired fundamental concepts of stochastic processes.
- Learn some of the most important stochastic processes used in practice to model random phenomena,

UNIT I

ID TRANSFORMS:

Review of Fourier analysis - Analysis of different periodic & non periodic waveforms – Sampling Theorem -DFS - DTFT - DFT - inverse DFT- properties - FFT – radix r algorithm – DIT FFT & DIF FFT - Convolution – reviewof Z transform- Hilbert transform.

UNIT II

2D TRANSFORMS:

Need for transform – 2D Orthogonal and Unitary transform and its properties – 2D DFT – Properties – FFT –Statement , proof and properties of Separable

transforms – Walsh, Hadamard, Haar, Discrete Sine, DCT, Slant, SVD & KL transforms.

UNIT III

WAVELET TRANSFORMS:

Wavelet transforms – 1D & 2D Wavelet transform – Time and frequency decompositions – STFT – Continues and discrete – CWT, DWT , Harr wavelet and Shannon wavelet– Fast Wavelet transform – Wavelet Packets.

UNIT IV

PROBABILITY & RANDOM VARIABLES:

Probability concepts- Random variable – moment generating function – discrete types, continues types -2D variable random variables – marginal, conditional, joint probability distribution – Binomial, Poisson, uniform, normal and Exponential distributions.

UNIT V

RANDOM PROCESS – 1:

Notion of stochastic processes , Auto Correlation – Cross Correlation – WSS – Ergodicity - power spectral density function – properties - Discrete random process – expectations – variance , co variance – scalar product – energy of discrete signals – Parseval's theorem.

UNIT VI

RANDOM PROCESS – 2:

Wiener Khintchine relation –- Discrete random signal processing by linear systems - response of linear discrete systems to white noise - Two dimensional random variables – transformation of random variables - regression system - simulation of white noise – low pass filtering of white noise.

TEXT BOOK:

1. Ronald W. Schafer, Alan V. Oppenheim, Discrete Time Signal Processing", Prentice Hall 3rd Edition, 2009.

REFERENCE BOOKS:

1. Gonzalez, Woods and Eddins, “Digital Image Processin” Prentice Hall, 3rd Edition, 2008.

2. Raghuveer M. Rao, Ajith S. Bopardikar, “Wavelet Transform: Introduction to theory & Applications; Prentice Hall 1st Edition, 1998.

3. Yaglon.A.M “Probability and information”, Springer Publication- 1983

4. W. John Wodds “Probability and random process with application to signal processes” Prentice Hall-2001

5. Atkinson.F.V “Discrete and continuous boundary problems”, Academic Press Inc -volume 8 -1998

HDL PROGRAMMING LABORATORY

(Common to VLSI and DECS)

SUBJECT CODE: 13MVL1101

L	P	C	INT	EXT
0	4	2	40	60

COURSE OBJECTIVES:

- To develop, analyze and experience with principle of designing digital circuits.

COURSE OUTCOMES:

- The students can simulate, synthesis and implement the digital circuits by using VHDL/Verilog and FPGA/CPGA devices.

The students are required to simulate, synthesize and implement the following experimental part, on the VHDL/Verilog environment.

1. Digital Circuits Description using Verilog and VHDL
2. Verification of the Functionality of Designed circuits using function Simulator.
3. Timing simulation for critical path time calculation.
4. Synthesis of Digital circuits
5. Place and Route techniques for major FPGA vendors such as Xilinx, Altera and Actel etc.
6. Implementation of Designed Digital Circuits using FPGA and CPLD devices.

DSP PROCESSORS AND ARCHITECTURES

(Common to VLSI and DECS)

SUBJECT CODE: 13MVL1009

L	P	C	INT	EXT
4	0	3	40	60

COURSE OBJECTIVES:

- To have an overview of digital signal processing.
- To study the design of various building blocks of DSP processors.
- To study the designing of programmable DSP processors.

COURSE OUTCOMES:

- At the end of the course, the student will be able to:
- Understand required building blocks to design a DSP processors.
- Understand different DSP processors and basic programming skills.

UNIT – I

INTRODUCTION TO DIGITAL SIGNAL PROCESING:

Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.

UNIT – II

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS:

Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT – III

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES:

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

EXECUTION CONTROL AND PIPELINING:

Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT – IV

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS:

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT – V

IMPLEMENTATIONS OF BASIC DSP AND FFT ALGORITHMS:

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

UNIT – VI

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES:

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS:

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.

2. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. S. Chand & Co, 2000.

REFERENCE BOOKS:

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkata Ramani and M. Bhaskar, TMH, 2004.

2. Digital Signal Processing – Jonatham Stein, John Wiley, 2005

WIRELESS COMMUNICATION & NETWORKS

SUBJECT CODE: 13MDE1004

L	P	C	INT	EXT
4	0	3	40	60

COURSE OBJECTIVES:

- This course emphasizes the description, modeling and performance evaluation of the physical and medium access control layers of the wireless personal area network.

COURSE OUTCOMES:

- Understand the fundamentals of wireless networking.
- Understand Wireless Local Area Networks & their performance analysis.

UNIT – I

INTRODUCTION TO WIRELESS NETWORKING:

Introduction, Difference between wireless and fixed telephone networks, Development of wireless networks, Traffic routing in wireless networks. Wireless data services: CDPD, ARDIS, RMD, Common channel signaling, ISDN, BISDN and ATM, SS7, SS7 user part, signaling traffic in SS7.

UNIT – II

MULTIPLE ACCESS TECHNIQUE & MAC CHANNELS FOR WIRELESS COMMUNICATION:

Introduction, TDMA, FDMA, CDMA, SDMA ,Packet radio, Packet radio protocols, CSMA protocols, Reservation protocols, MAC channels, MAC channel capacity with fading and ISI.

UNIT – III

FUNDAMENTAL CONCEPTS OF SPREAD SPECTRUM SYSTEMS:

pseudo noise sequence, analysis of DSSS systems - the processing gain and anti jamming margin - frequency hopped spread spectrum systems - time hopped spread spectrum systems - synchronization of spread spectrum systems

UNIT – IV

MOBILE IP AND WIRELESS ACCESS PROTOCOL:

Operation of mobile IP, Co-located address, Registration, Tunneling, WAP Architecture, WAP service, WAP session protocol, wireless transaction, Wireless datagram protocol.

UNIT – V

WLAN TECHNOLOGY:

Infrared LANs, Spread spectrum LANs, Narrow bank microwave LANs.

UNIT – VI

BLUE TOOTH AND MOBILE DATA NETWORKS:

Overview, Radio specification, Base band specification, Links manager specification, Logical link control and adaptation protocol, Mobile data networks Introduction, Wireless ATM, HIPERLAN, Adhoc Networking and WPAN.

TEXT BOOKS:

1. Wireless Communications, Principles, Practice – Theodore, S. Rappaport, PHI, 2nd Edn., 2002.

2. Wireless Communication and Networking – William Stallings, PHI, 2003.

REFERENCE BOOKS:

1. Wireless Digital Communications – Kamilo Feher, PHI, 1999.

2. Principles of Wireless Networks – Kaveh Pah Laven and P. Krishna Murthy, Pearson Education, 2002.

3. Wireless Communications – Andreaws F. Molisch, Wiley India, 2006.

4. Introduction to Wireless and Mobile Systems – Dharma Prakash Agarwal, Qing-An Zeng, Thomson 2nd Edition, 2006.

OPTICAL COMMUNICATION

SUBJECT CODE: 13MDE1005

L	P	C	INT	EXT
4	0	3	40	60

COURSE OBJECTIVES:

- To get insight into different fiber types, fabrication methods, optical transmission characteristics, optical sources, optical detectors and optical amplifiers.
- To understand different design considerations in optical links involving link power budget and rise time budget.

COURSE OUTCOMES:

- Learner will apply knowledge of mathematics to solve numerical based on step index and graded index fibers.
- Students will understand fiber performance parameters like NA, Group delay, Phase and Group velocity .They will understand optical transmission characteristics theoretically and practically.
- Learners will understand analog and digital links, design consideration of optical links, WDM, fiber data transfer rates in social context.

UNIT –I

OVERVIEW OF OPTICAL FIBER COMMUNICATIONS:

The evolution of fiber optic systems, elements of an optical fiber transmission link. Advantages of optical fiber communication, applications. Optical Fibers: structures, wave guiding, Nature of light, Basic optical laws and definitions, optical fiber modes and configurations (Fiber types, Rays and modes, step index and graded index fibers). mode theory of circular waveguides.

UNIT – II

OPTICAL SOURCES:

LEDs, structures, quantum efficiency, modulation capability, Laser diodes: Laser diodes and threshold conditions, external quantum efficiency resonant frequencies, laser diode structures and radiation pattern, temperature effects, reliability.

UNIT – III

PHOTO DETECTORS:

Physical principles of photodiodes (pin Photodiode, avalanche, photo diode) comparison of photo detectors, noise in detectors.

UNIT –IV

FABRICATION, CABLING AND INSTALLATION:

Fabrication, fiber optic cables, Installation- placing the cable. Optical Communication Systems: Block diagrams of optical communication systems, direct intensity modulation, digital communication systems, Laser semiconductor transmitter, Generations of optical fiber link, description of 8 Mb/s optical fiber communication link, description of 2.5 Gb/s optical fiber communication link.

UNIT – V

COMPONENTS OF FIBER OPTIC NETWORKS – 1:

Overview of fiber optic networks, Transreceiver, semiconductors optical amplifiers, couplers/splicers, wavelength division multiplexers and demultiplexers, filters, isolators and optical switches.

UNIT – VI

COMPONENTS OF FIBER OPTIC NETWORKS – 2:

Basic Fiber Optic networks, SONET/SDIT, Broad cast and select WDM Networks, wavelength routed networks, optical CDMA. Optical Sensors, Optical Amplifiers (EDFA, ROMAN)

TEXT BOOKS:

1.Optical fiber communications – Gerd Keiser, 3 rd Ed. MGH.

2.Fiber Optic Communication Technology – Djafar K. Mynbaev and Lowell L. Scheiner, (Pearson Education Asia)

3.Optoelectronic devices and systems – S.C. Gupta, PHI, 2005.

REFERENCE BOOKS:

1.Fiber Optics Communications – Harold Kolimbiris (Pearson Education Asia)

2. Optical Fiber Communications and its applications – S.C. Gupta (PHI) 2004.

3.WDM Optical Networks – C. Siva Ram Murthy and Mohan Guru Swamy, PHI.

4.Fiber Optic communications – D.C. Agarwal, S.Chand Publications, 2004

CODING THEORY & PRACTICE

SUBJECT CODE: 13MDE1006

L	P	C	INT	EXT
4	0	3	40	60

COURSE OBJECTIVES:

- Learn fundamentals of wireless channel characteristics and coding methods .
- Understand various channel coding methods, their performance and applications.

COURSE OUTCOMES:

- Understand about the need and importance of channel coding methods.
- The student can able to apply various coding and can evaluate their performance.

UNIT – I

INTRODUCTION:

Digital communication system, Wireless channel statistical models, BER performance in AWGN and fading channels for different modulation schemes, BER performance of CDMA, FH – CDMA in AWGN and fading channels, capacity of fading channels with CSI, Diversity reception, channel coding Theorem, Channel coding gain.

UNIT – II

BLOCK CODING:

Galois fields, polynomials over Galois fields, RS codes, Decoding Techniques for RS codes, LDPC encoder and decoder, Performance analysis of RS and LDPC codes. BCH codes.

UNIT – III

CONVOLUTION CODES – 1:

Linear convolution encoders, Structural properties of Convolution codes.

UNIT – IV

CONVOLUTION CODES – 2:

Viterbi decoding technique for convolution codes – Soft / Hard decision, concatenation of block codes and convolution codes, performance analysis, concept of Trellis coded modulation.

UNIT – V

TURBO CODES:

Parallel concatenation, Turbo encoder, Iterative decoding using BCJR algorithm, Performance analysis.

UNIT – VI

SPACE – TIME CODING:

MIMO systems, MIMO fading channels, rate gain & diversity gain, transmit diversity, Alamouti scheme, OSTBC codes, Linear space – time codes, trellis space – time codes, Space – time codes with no CSI.

TEXT BOOKS:

1. S.B. Wicker, Error control systems for Digital communication and storage, Prentice-hall 1995.

2. E. Biglieri, Coding for Wireless Channels, Springer,2007.

3. K.L.Du & M.N.S.Swamy, Wireless Communication Systems: From RF Subsystems to 4G Enabling Technoligies, Cambridge,2010.

4. J.G. Proakis & M. Salehi, Digital Communications, Mc Graw-Hill, 2008.

SYSTEM MODELING & SIMULATION

(Common to VLSI and DECS)(Elective-III)

SUBJECT CODE: 13MVL1013

L	P	C	INT	EXT
4	0	3	40	60

COURSE OBJECTIVES:

- The main objective of this course is to introduce basic concept of modeling and simulation of discrete events and systems.

COURSE OUTCOMES:

- Able to understand the concept of modeling, analysis and simulation of discrete events and systems.

UNIT – I

BASIC SIMULATION MODELING:

Systems, Models and Simulation, Discrete Event Simulation, Simulation of Single server queuing system, Simulation of Inventory System, Alternative approach to modeling and simulation.

UNIT – II

SIMULATION SOFTWARE:

Comparison of simulation packages with Programming Languages, Classification of Software, Desirable Software features, General purpose simulation packages – Arena, Extend and others, Object Oriented Simulation, Examples of application oriented simulation packages.

UNIT – III

BUILDING SIMULATION MODELS:

Guidelines for determining levels of model detail, Techniques for increasing model validity and credibility.

MODELING TIME DRIVEN SYSTEMS:

Modeling input signals, delays, System Integration, Linear Systems, Motion Control models, numerical experimentation.

UNIT – IV

EXOGENOUS SIGNALS AND EVENTS:

Disturbance signals, state machines, petri nets & analysis, System encapsulation.

MARKOV PROCESS:

Probabilistic systems, Discrete Time Markov processes, Random walks, Poisson processes, the exponential distribution, simulating a poison process, Continuous – Time Markov processes.

UNIT – V

EVEN DRIVEN MODELS:

Simulation diagrams, Queuing theory, simulating queuing systems, Types of Queues, Multiple Servers.

UNIT – VI

SYSTEM OPTIMIZATION:

System identification, Searches, Alpha/beta trackers, multidimensional optimization, modeling and simulation methodology.

TEXT BOOKS:

1. System Modeling & Simulation, An introduction – Frank L.Severance, John Wiley&Sons, 2001.

2. Simulation Modeling and Analysis – Averill M.Law, W.David Kelton, TMH, 3rd Edition, 2003.

REFERENCE BOOK:

Systems Simulation – Geoffery Gordon, PHI, 1978.

RADAR SIGNAL PROCESSING

(Elective-III)

SUBJECT CODE: 13MDE1007

L	P	C	INT	EXT
4	0	3	40	60

COURSE OBJECTIVES:

- Learn the fundamental issues involved in radar signal processing.
- Learn the frequency and time domain methods of power and velocity measurements.
- Learn algorithms for the enhancement of radar performance.
- Learn how a Doppler radar can be used for precipitation measurements.
- Study the statistical properties of the various algorithms used with Doppler radars.

COURSE OUTCOMES:

- Able to understand the concepts, analysis and processing of radar signals with and without noise.

UNIT-I

INTRODUCTION:

Classification of Radars based on functions, principles of operation etc., performance measures and interplay between Radar parameters, Target parameters and Environment parameters. Classical Detection and Estimation Theory, Binary Hypotheses Testing, Likelyhood Ratio Test, Neymon square, MAP, Maximum Likelihood Estimation of parameters, Cramer-Rao Bounds, Chemoof Bounds.

UNIT – II

REPRESENTATION OF SIGNALS:

K-L expansion, Equivalent Low-pass representation of Band pass signals and noise. Detection of Slowly Fluctuating point Targets in white noise and coloured noise. Swerling Target models.

UNIT – III

OPTIMUM RECEIVERS:

Correlator and Band pass M atohed Filter Receivers. PD – PF performance, Coherent and non-coherent Integration sub-optimum Reception. Radar Power – Aperture product.

UNIT – IV

RANGE AND DOPPLER RESOLUTION:

Ambiguity function and its properties. Local and Global Accuracy. Signal Design. LFM. Polyphase coded signals Detection of a Doppler shifted slowly fluctuating point target return in a discrete scatterer environment.

UNIT – V

Dobly 47ispersive Fading Target and Clutter models-Scattering function description. Land clutter-pulse length limited and Beam width limited clutter. Sea clutter.

UNIT – VI

Optimum / Sub optimum reception of Range Spread / Doppler Spread / Doubly spread targets in the presence of noise and clutter. Introduction to Adaptive Detection and CFAR Techniques.

TEXT BOOKS:

1. Di Franco. JV and Rubin, WL., "Radar Detection", Artech House, 1980.

2. Gaspare Galati (Ed), "Advanced Radar Techniques and Systems", Peter Perigrinus Ltd., 1993.

3. Ramon Nitzberg, "Radar Signal Processing and Adaptive Systems", Artech House, 1999.

4. August. W Rihaczek, "Principles of High Resolution Radar", Artech House, 1996.

IMAGE AND VIDEO PROCESSING

(Elective-IV)

SUBJECT CODE: 13MDE1008

L	P	C	INT	EXT
4	0	3	40	60

COURSE OBJECTIVES:

- This course provides an introduction to the basic concepts and techniques used in digital image and video processing. Two-dimensional sampling and quantization are studied, and the human visual system is reviewed. Edge detection and feature extraction algorithms are introduced for dimensionality reduction and feature classification. High-pass and bandpass spatial filters are studied for use in image enhancement. Applications are discussed in frame interpolation, filtering, coding, noise suppression, and video compression.

COURSE OUTCOMES:

- On completion of this course the student shall have comprehension of the technologies and issues related to content-based indexing and retrieval solutions and shall have understanding of the challenges and limitations of content-based indexing and retrieval systems.
- The student shall be able to identify and evaluate the use of content-based features in indexing and retrieval of various types of media content (such as text, images, audio, and video).
- The student shall be able to evaluate and compare alternative content-based retrieval indexes and similarity measures.

UNIT I

FUNDAMENTALS OF IMAGE PROCESSING AND IMAGE TRANSFORMS:

Basic steps of Image Processing System, Sampling and Quantization of an image, relationship between pixels.

IMAGE TRANSFORMS:

2 D- Discrete Fourier Transform, Discrete Cosine Transform (DCT), Wavelet Transforms: Continuous Wavelet Transform, Discrete Wavelet Transforms.

UNIT II

IMAGE PROCESSING TECHNIQUES – 1: (Image Enhancement)

Spatial domain methods: Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters.

Frequency domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, Selective filtering.

UNIT III

IMAGE PROCESSING TECHNIQUES – 1: (Image Segmentation)

Segmentation concepts, Point, Line and Edge Detection. Thresholding, Region Based segmentation.

UNIT IV

IMAGE COMPRESSION:

Fundamentals - Coding Redundancy, Spatial and Temporal redundancy.

Compression models: Lossy & Lossless, Huffman coding, Arithmetic coding, LZW coding, Run length coding, Bit plane coding, Transform coding, Predictive coding, Wavelet coding, JPEG Standards.

UNIT V

BASIC CONCEPTS OF VIDEO PROCESSING:

Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, filtering operations.

UNIT VI

2-D MOTION ESTIMATION:

Optical flow, General Methodologies, Pixel Based Motion Estimation, Block-Matching Algorithm, Mesh based Motion Estimation, Global Motion

Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

TEXT BOOKS:

1. Gonzaleze and Woods ,Digital Image Processing , 3rd ed., Pearson.

2. Yao Wang, Joem Ostermann and Ya–quin Zhang ,Video processing and communication, 1st Ed., PH Int.

3. M. Tekalp ,Digital Video Processing , Prentice Hall International

NETWORK SECURITY AND CRYPTOGRAPHY

(Common to VLSI and DECS)(Elective-IV)

SUBJECT CODE: 13MVL1016

L	P	C	INT	EXT
4	0	3	40	60

COURSE OBJECTIVES:

- Learn fundamentals of cryptography and its application to network security.
- Understand network security threats, security services, and countermeasures.
- Acquire background on well known network security protocols.
- Understand vulnerability analysis of network security.

COURSE OUTCOMES:

- Understand network security and cryptography concepts and applications.
- The student can able to apply security principles to system design.
- Identify and investigate network security threats.
- Analyze and design network security protocols.

UNIT – I

SYMMETRIC CIPHERS:

Overview – classical Encryption Techniques, Block Ciphers and the Data Encryption standard, Introduction to Finite Fields, Advanced Encryption standard, Contemporary Symmetric Ciphers, Confidentiality using Symmetric Encryption.

PUBLIC-KEY ENCRYPTION AND HASH FUNCTIONS:

Introduction to Number Theory, Public-Key Cryptography and RSA, Key Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication and Hash Functions, Hash Algorithms, Digital Signatures and Authentication Protocols.

UNIT – II

NETWORK SECURITY PRACTICE:

Authentication Applications, Kerbors, X.509 Authentication Service, Electronic mail Security, Pretty Good Privacy, S/MIME, IP Security architecture, Authentication Header, Encapsulating Security Payload, Key Management.

UNIT – III

SYSTEM SECURITY:

Intruders, Intrusion Detection, Password Management, Malicious Software, Firewalls, Firewall Design Principles, Trusted Systems.

WIRELESS SECURITY:

Introduction to Wireless LAN Security Standards, Wireless LAN Security Factors and Issues.

UNIT – IV

ENCRYPTION TECHNIQUES:

Conventional techniques, Modern techniques, DES, DES chaining, Triple DES, RSA algorithm, Key management, Message Authentication, Hash Algorithm, Authentication requirements, functions secure Hash Algorithm, Message digest algorithm, digital signatures, AES Algorithms.

UNIT – V

SECURE NETWORKING THREATS:

Attack Process, Attacker Types. Vulnerability Types, Attack Results, Attack Taxonomy, Threats to Security, Physical security, Biometric systems, monitoring controls, Data security, intrusion, detection systems.

UNIT – VI

DESIGNING SECURE NETWORKS:

Components of a Hardening Strategy, Network Devices, Host Operating Systems, Applications, Based Network Services, Rogue Device Detection, Network Security Technologies, the Difficulties of Secure Networking, Security

Technologies, Emerging Security Technologies General Design Considerations, Layer 2 Security Considerations, IP Addressing Design Considerations - ICMP Design Considerations, Routing Considerations, Transport Protocol Design Considerations.

TEXT BOOKS:

1. William Stallings, "Cryptography and Network Security – Principles And Practices", Pearson Education, 3rd Edition, 2003.

2. Sean Convery, " Network Security Architectures, Published by Cisco Press, First Ed. 2004.

REFERENCES BOOKS:

1. Atul Kahate, "Cryptography and Network Security", Tata McGraw Hill, 2003.

2. Bruce Schneier, "Applied Cryptography", John Wiley and Sons Inc, 2001.

3. Stewart S. Miller, "Wi-Fi Security", McGraw Hill, 2003.

4. Charles B. Pfleeger, Shari Lawrence Pfleeger, "Security In Computing", 3rd Edition, Pearson Education, 2003.

5. Jeff Crume, "Inside Internet Security" Addison Wesley, 2005.

DIGITAL SIGNAL, IMAGE AND VIDEO PROCESSING LAB

SUBJECT CODE: 13MDE1101

L	P	C	INT	EXT
0	4	2	40	60

COURSE OBJECTIVES:

- Understand the basic digital signal, image and video processing algorithms and their implementation in C or MATLAB.

COURSE OUTCOMES:

- Understand the fundamentals of image and video signal processing and associated techniques.
- Understand how to solve practical problems with some basic image and video signal processing techniques.
- Have the ability to design simple systems for realizing some multimedia applications with some basic image and video signal processing techniques.

The students are required to simulate the following experimental parts on the MATLAB environment by consider the relevant application based examples.

PART-1: Digital Signal Processing

1. Discrete-time Signals and Systems in the time domain.
2. z-Transforms and inverse z-Transforms.
3. The Discrete Fourier Transform properties.
4. FIR Filter Design.
5. IIR Filter Design.
6. Applications in Adaptive Filtering.

PART-2: Image Processing

1. Image Enhancement in Spatial Domain
2. Fourier Transform of an Image
3. Enhancement in Frequency Domain.
4. Image segmentation
5. Image Compression.

PART-3: Video Processing

1. Divide 1sec video into frames
2. Filter operations on video(Smoothing and Sharpening)
3. Motion estimate of an object in a video.