AR22

COURSE STRUCTURE AND SYLLABI

FOR

M.TECH

VLSI SYSTEM DESIGN

From The Academic Year 2022 – 2023

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT
(An Autonomous Institution)
Approved by AICTE, Permanently Affiliated to JNTUGV, Vizianagaram
Accredited by NBA & NAAC, Recognized by UGC under 2(f) & 12(b)
K. Kotturu, TEKKALI – 532 201, Srikakulam Dist., A.P.,

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT (AUTONOMOUS)

Approved by AICTE, Accredited by NBA & NAAC, Recognised under 2(f)12(b) of UGC,
Permanently Affiliated to JNTUGV, Vizianagaram.
K.Kotturu, Tekkali, Srikakulam-532201, Andhra Pradesh

Academic Regulations for M.Tech

(Effective for the students admitted into first year from academic year 2022-2023)

The M.Tech Degree of the Aditya Institute of Technology and Management (Autonomous), Tekkali shall be conferred on candidates who are admitted to the program and fulfill all the requirements for the award of the Degree.

1.0 ELIGIBILITY FOR ADMISSIONS:

Admission to the above program shall be made subject to the eligibility, qualifications and specialization prescribed by the University from time to time. Admissions shall be made on the basis of merit / rank obtained by the qualifying candidate in GATE / PGCET, subject to reservations prescribed by the Govt. of AP from time to time.

2.0 AWARD OF M. Tech DEGREE:

2.1 A student shall be declared eligible for award of the M.Tech degree, if he/she pursues a course of study and completes it successfully in not less than two academic years and not more than four academic years.

2.2 A student, who fails to fulfill all the academic requirements for the award of the degree within four academic years from the year of his/her admission, shall forfeit his/her seat in M.Tech course.

2.3 The student shall register for all 68 credits and secure all the 68 credits.

3.0 ATTENDANCE:

3.1 The minimum instruction for each semester 90 clear instruction days.

3.2 A candidate shall be deemed to have eligibility to write End Semester examinations if he/she has put in a minimum of 75% of attendance in aggregate of all the subjects.

3.3 Condonation of shortage of attendance up to 10% (65% and above, and below 75%) may be given by the College academic committee.

3.4 Condonation of shortage of attendance shall be granted only on genuine and valid reasons on representations by the candidate with supporting evidence.

3.5 Shortage of attendance below 65% shall in NO case be condoned.

3.6 A candidate shall not be promoted to the next semester unless he/she fulfills the attendance requirements of the present semester.

3.7 A stipulated fee shall be payable towards condonation of shortage of attendance.

4.0 COURSE OF STUDY:

The following specializations are offered at present for the M.Tech course of study.

1	VLSI System Design
2	Power Electronics and Drives
3	Computer Science and Engineering
4	Structural Engineering
5	Thermal Engineering

4.1 A standard academic format common for all PG programmes describing numbers of credits, weightage for lecture, laboratories work and projects have been fixed considering the scope of study. The position and sequence of study of core courses and elective courses are made to ensure sequential and integral learning. The focus on advance study in core courses through theory and laboratories work supported by study on relevant programme specific electives are incorporated. The selection of unique courses in the basket of elective is a special feature of curriculum ensuring flexibility and diversity. The emphasis on understanding advanced Concepts of PG course is ensured through elaborate practical work conducted through actual/virtual laboratory experiments. The concept of designing experiments and developing concept

application is made part of learning process. The PG course is spread over two years in four semesters and inclusion of Minor project, Audit course, Open elective, Technical Seminar and Dissertation are the special features of this curriculum. The contents of course are unitised to facilitate its execution. The list of suggested reading is also made part of the curriculum.

4.2 The students are asked to learn IPR/ research methodology to understand the importance and process of creation of patents through research. The introduction of One Audit course covering subjects of developing desired attitude among the Learners is on the line of initiatives such as English for research paper writing, Disaster management, and Constitution of India and Personality development through life enlightenment skills. The courses included under open electives are of importance in the context of special skill development and they are on Industrial safety, Operation research, Composite materials and Waste to Energy. These courses shall make students capable to work in industrial environment.

4.3 The introduction of Minor project ensures preparedness of students to undertake major projects/ dissertation. Students are encouraged to go to Industrial Training/Internship for at least 2-3 months during semester break. The dissertation/major project work of PG programme of one-year duration is given strong weightage in the curriculum. It is expected to undertake industrially relevant problem to develop an optimal solution through extensive research work. The students and faculty can design the research project in consultation with industry preferably in the region.

5.0 EVALUATION:

The performance of the candidate in each semester shall be evaluated subject-wise with a maximum of 100 marks for theory and 100 marks for laboratory, on the basis of continuous Internal Evaluation and Semester End Examination.

5.1 For Theory Courses, **40** marks shall be for internal evaluation and **60** marks for end semester examination. Out of **40** internal marks **30** marks are assigned for subjective exam, **5** marks for assignments and **5** marks for seminars. The internal evaluation for **30** marks shall be made based on the average of the marks secured in the two Mid Term-Examinations conducted, one in the middle of the Semester and the other immediately after the completion of instruction. Each

midterm examination shall be conducted for duration of **120** minutes and question paper shall contain **4** questions. The student should answer all **4** questions.

5.2 For courses like **Research Methodology & IPR** and **Open Elective,** the pattern of midterm and end examinations is similar to regular theory courses and the valuation is purely internal. Evaluation is based on continuous assessment.

5.3 Audit course is one among the compulsory courses and does not carry any Credits and no semester end examination.

5.4 For laboratory courses, **40** marks shall be for internal evaluation and **60** marks for end semester examination. Out of **40** internal marks **20** marks are assigned based on day-to-day evaluation and **20** are assigned based on the internal test. The end examination shall be conducted by the teacher concerned and an external examiner.

5.5 For Minor Project, **40** marks shall be for internal evaluation and **60** marks for end semester examination. The end semester examination (Viva-Voce) shall be conducted by a committee. The committee consists of an External examiner, Head of the department and Supervisor of the minor project. The internal evaluation shall be made on the basis of seminar given by each student on the topic of his/her minor project, which was evaluated by Departmental committee. The Departmental Committee consists of Head of the Department, supervisor and one other senior faculty member from the Department. Out of **40** internal marks **10** marks allotted for literature survey, **15** marks for results and analysis and **15** marks for seminar.

5.6 For Technical Seminar there will be only internal evaluation for **100** marks. A candidate has to secure a minimum of **50%** marks to be declared successful. For evaluation the candidate has to collect literature on a topic, prepare the document, submit it to the Department in a report form and shall make an oral presentation before the Departmental Committee. The Departmental Committee consists of Head of the Department and two other senior faculty members from the department.

5.7 A candidate shall be deemed to have secured the academic requirement in a subject if he/she secures a minimum of 40% of marks in the end semester examination and a minimum aggregate

of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

5.8 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 5.7) he has to reappear for the supplementary examination in that subject in the next academic year.

6.0 EVALUATION OF DISSERTATION Phase – 1/DISSERTATION Phase – 2 WORK:

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the Dissertation Review Committee.

6.1 A DISSERTATION Review Committee (DRC) shall be constituted with Principal as chair Person, Head of the department, Supervisor and one senior faculty member of the concerned department.

6.2 Registration of DISSERTATION: A candidate is permitted to register for the Dissertation after satisfying the attendance requirement of all the subjects (theory and practical subjects) in Second semester.

6.3 After satisfying 6.2, a candidate has to submit, in consultation with his supervisor, the title, objective and plan of action of his dissertation work to the Dissertation Review Committee for its approval. After obtaining the approval of the Committee the student can initiate the dissertation work after the second semester end examinations.

6.4 Every candidate shall work on dissertation approved by the DRC of the Department.

6.5 If a candidate wishes to change his supervisor or topic of the dissertation he can do so with approval of the DRC. However, the Dissertation Review Committee (DRC) shall examine whether the change of topic/supervisor leads to a major change of his initial plans of project proposal. If so, his date of registration for the dissertation work starts from the date of change of Supervisor or topic as the case may be.

6.6 A candidate shall submit status report in two stages at least with a gap of 3 months between them.

6.7 The work on the dissertation shall be initiated in the beginning of the III semester and the duration of the dissertation is for two semesters. The candidate shall identify the problem, Literature survey, design/modeling part of the problem i.e. almost 35% of his dissertation work should be completed in the III semester itself and it will be evaluated by DRC as Dissertation Phase – 1. If the candidate fails to get the satisfactory report, he has to re-register for the dissertation work.

6.8 A candidate shall be allowed to submit the dissertation report only after fulfilling the attendance requirements of all the semesters with approval of DRC and not earlier than 40 weeks from the date of registration of the dissertation work. For the approval of DRC the candidate shall submit the draft copy of dissertation to the Principal (through Head of the Department) and shall make an oral presentation before the DRC.

6.9 The Candidate may be permitted to submit the Dissertation Report, if only the student pass in all subjects and work is Published/Accepted to be published in a Journal / International conference of repute and relevance.

6.10 Three copies of the Dissertation Report certified by the Supervisor shall be submitted to the College.

6.11 The Dissertation shall be adjudicated by external examiner from outside the college.

6.12 The viva-voce examination shall be conducted by a board consisting of the Supervisor, Head of the Department and the examiner outside the college.

The Board shall jointly report candidates work as:

A. Excellent
B. Good
C. Satisfactory
D. Unsatisfactory

Head of the Department shall coordinate and make arrangements for the conduct of viva-voce examination. If the report of the viva-

voce is unsatisfactory, the candidate will retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second viva-voce examination, the candidate may be asked to submit a new Dissertation proposal to DRC starting with 6.4

7. Method of Awarding Letter Grades and Grade Points for a Course:

A letter grade and grade points will be awarded to a student in each course based on his/her performance as per the grading system given below.

Table: Grading System for M.Tech. Programme

Percentage	Level	Letter Grade	Grade Points
>= 90%	Outstanding	A+	10
80 to <90%	Excellent	A	9
70 to <80%	Very Good	B	8
60 to <70%	Good	C	7
50 to <60%	Fair	D	6
< 50%	Fail	F	0
-	Absent	AB	0

7.1 Calculation of Semester Grade Points Average (SGPA)* for semester

The performance of each student at the end of the each semester is indicated in terms of SGPA. The SGPA is calculated as below:

$$\text{SGPA} = \frac{\Sigma(\text{CR} \times \text{GP})}{\Sigma\text{CR}}$$ (for all courses passed in semester)

Where CR = Credits of a Course
GP = Grade points awarded for a course

SGPA is calculated for the candidates who passed all the courses in that semester.

7.2 Calculation of Cumulative Grade Points Average (CGPA) and Award of Division for Entire Programme.

The CGPA is calculated as below:

$$CGPA = \frac{\Sigma(CR \times GP)}{\Sigma CR}$$ (for entire programme)

Where CR = Credits of a course

GP = Grade points awarded for a course

CGPA is calculated for the candidates who passed all the courses till that semester.

As per the AICTE regulations, conversion of CGPA into equivalent percentage as follows:

Equivalent Percentage = (CGPA – 0.75) x 10

After a student has satisfied the requirement prescribed for the completion of the programme and is eligible for receiving the award of M.Tech. Degree, he shall be placed in one of the below divisions:

Table: Award of Divisions

Class Awarded	CGPA Secured	Remarks
First Class with distinction	≥ 7.75 (Without any supplementary appearance)	From the CGPA secured from 68 Credits
First Class	≥ 6.75	
Second Class	≥ 6.0 and < 6.75	

8.0 WITH-HOLDING OF RESULTS:

If the candidate has not paid any dues to the college or if any case of indiscipline is pending against him / her, the result of the candidate will be withheld and he/she will not be allowed into the next higher semester. The issue of the degree is liable to be withheld in such cases.

9.0 TRANSITORY REGULATIONS:

Candidate who have discontinued or have been detained for want of attendance or who have failed after having undergone the course are eligible for admission to the same or equivalent subjects as and when subjects are offered, subject to 5.8 and 2.0.

10.0 GENERAL:

10.1 The academic regulations should be read as a whole for purpose of any Interpretation.

10.2 In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Principal is final.

10.3 The Institute may change or amend the academic regulations and syllabus at any time and the changes and amendments made shall be applicable to all the students with effect from the date notified by the college.

10.4 Wherever the word he, him or his occur, it will also include she, her and hers.

* * * * *

Aditya Institute of Technology and Management, Tekkali M.Tech. – VLSI System Design

(AR22 Regulations)

COURSE STRUCTURE

M. Tech. (VLSI System Design) – 1st SEMESTER						
S.NO.	**SUBJECT CODE**	**SUBJECT**	**L**	**T**	**P**	**C**
1	22MVL1001	Digital Design through HDL	3	0	0	3
2	22MVL1002	Digital Signal and Image Processing	3	0	0	3
3	**Elective – I**					
	22MVL1003	VLSI Technology & Design	3	0	0	3
	22MVL1004	CMOS Analog IC Design				
	22MVL1005	DSP Processors and Architecture				
4	**Elective – II**					
	22MVL1006	VLSI Signal Processing	3	0	0	3
	22MVL1007	Digital System Design				
	22MVL1008	Embedded system design				
5	22MVL1101	HDL Programming Lab	0	0	4	2
6	22MVL1102	Digital Signal and Image Processing Lab	0	0	4	2
7	22MCC1001	Research Methodology and IPR	2	0	0	2
8	**Audit Course**					
	22MAC1001	English for Research Paper Writing	2	0	0	0
	22MAC1002	Disaster Management				
	22MAC1003	Constitution of India				
	22MAC1004	Personality Development through Life Enlightenment Skills				
		TOTAL	16	0	8	18

M. Tech. (VLSI System Design) – 2nd SEMESTER						
S.NO.	**SUBJECT CODE**	**SUBJECT**	**L**	**T**	**P**	**C**
1.	22MVL1009	Mixed Signal IC Design	3	0	0	3
2.	22MVL1010	Design of Fault Tolerant Systems	3	0	0	3
3.	**Elective – III**					
	22MVL1011	Low Power VLSI Design	3	0	0	3
	22MVL1012	CAD of Digital Systems				
	22MVL1013	Memory Technologies				
4.	**Elective – IV**					
	22MVL1014	Algorithms for VLSI Design Automation	3	0	0	3
	22M VL1015	CPLD and FPGA Architecture and Applications				
	22M VL1016	Communication buses and Interfaces				
5.	**Elective – V**					
	22MVL1017	System On Chip design	3	0	0	3
	22MVL1018	Hardware software co-design				
	22MVL1019	System Modeling & Simulation				

6.	**Open Elective:**					
	22MOE1001	Industrial Safety	3	0	0	3
	22MOE1002	Operations Research				
	22MOE1003	Composite Materials				
	22MOE1004	Waste to Energy				
7.	22MVL1103	Mixed Signal IC Design Lab	0	0	4	2
8.	22MVL1201	Minor Project	0	0	4	2
Total			18	0	8	22

M. Tech. (VLSI System Design) – 3rd SEMESTER						
S.NO.	**SUBJECT CODE**	**SUBJECT**	**L**	**T**	**P**	**C**
1	22MVL2202	Technical Seminar	-	-	-	2
2	22MVL2203	Dissertation Phase – 1	-	-	-	10
Total			-	-	-	12

M. Tech. (VLSI System Design) – 4th SEMESTER						
S. NO.	**SUBJECT CODE**	**SUBJECT**	**L**	**T**	**P**	**C**
1	22MVL2204	Dissertation Phase – 2	-	-	-	16
Total			-	-	-	16

NOTE: **L: Lecture** **T: Tutorial** **P: Practical**

Subject Code:

1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
Regulation		M	M. Tech Specialization		Year	Type of Subject	Subject Code	
22: AR22 Regulation		M: M.Tech	CS: Computer Science Engineering VL: VLSI System Design TE: Thermal Engineering PE: Power Electronics and Drives SE: Structural Engineering		1: 1st year 2: 2nd Year	0: Theory 1: Lab 2: Dissertation/Technical Seminar	0 0 0 0 0 0 0	1 2 3 4 5 6 7

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – I Sem.

DIGITAL DESIGN THROUGH HDL

Subject Code: 22MVL1001

L	T	P	C
3	0	0	3

Course Objectives:

- Learn the design and implement of the fundamental digital logic circuits using Verilog hardware description language.
- Find the design issues of system on chip.
- Write the Verilog & VHDL Programming for combinational circuits using different styles of modeling.
- Write the Verilog & VHDL Programming for sequential circuits using different styles of modeling.
- Design large Systems using tasks and functions.
- Design large systems using packages and libraries.

Course Outcomes:

At the end of this course, students will be able to

CO 1. Design and implement the fundamental digital logic circuits using Verilog & VHDL at various levels of abstractions.
CO 2. Develop the Test bench simulation programs for all logic circuits.
CO 3. Use the tasks and functions in digital system design process.
CO 4. Design a large digital systems based on small modules.
CO 5. Analyze the timing parameters of simulation and synthesis process.
CO 6. Analyze large systems using packages and libraries.

UNIT-I:

INTRODUCTION TO VERILOG : ASIC Design flow, FPGA Design flow, comparison between ASIC Design flow and FPGA Design flow, Features of Verilog HDL, different Levels of Design Description, Simulation, Test bench Simulation and Synthesis process,

LANGUAGE ELEMENTS OF VERILOG HDL: Introduction, Keywords, Identifiers, White Space Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Memory, Operators, System Tasks, Exercises.

UNIT-II:

GATE LEVEL MODELING : Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tri-State Gates, Array of Instances of Primitives, Additional Examples, Design of Flip flops with Gate Primitives, Delays, Strengths and Contention Resolution, Net Types, Design of Basic Circuits, Exercises.

UNIT-III:

BEHAVIORAL MODELING : Introduction, Operations and Assignments, Functional Bifurcation, Initial Construct, Always Construct, Examples, Assignments with Delays, Wait construct, Multiple Always Blocks, Designs at Behavioral Level, Blocking and Non blocking Assignments, The case statement, Simulation Flow. i*f* and i*f*-else constructs, assign-deassign construct, repeat construct, for loop, the disable construct, while loop, forever loop, parallel blocks, force-release construct, Event.

UNIT-IV:

MODELING AT DATA FLOW LEVEL: Introduction, Continuous Assignment Structures, Delays and Continuous Assignments, Assignment to Vectors, Operators. Verilog HDL programming for different combinational and sequential circuits.

SYSTEM TASKS, FUNCTIONS, AND COMPILER DIRECTIVES : Introduction, Parameters, Path Delays, Module Parameters, System Tasks and Functions, File-Based Tasks and Functions, Compiler Directives, Hierarchical Access, General Observations, Exercises, Function, Tasks, FSM Design (Moore and Mealy Machines)

UNIT-V:

INTRODUCTIONTO VHDL: BASIC LANGUAGE ELEMENTS: Identifiers, Data Objects, Data Types, And Operators.

BEHAVIORAL MODELING: Entity Declaration, Architecture Body, Process Statement, Variable Assignment Statement, Signal Assignment Statement, Wait Statement, If Statement, Case Statement, Null Statement, Loop Statement.

DATAFLOW MODELING: Concurrent Signal Assignment Statement, Concurrent versus Sequential Signal Assignment, Conditional Signal Assignment Statement.

UNIT-VI:

STRUCTURAL MODELING: Component Declaration, Component Instantiation, Examples, Resolving Signal Values.

GENERICS AND CONFIGURATIONS: Generics, Configuration Specification, Configuration Declaration.

PACKAGES AND LIBRARIES: Package Declaration, Package Body, Design Libraries, Design File.

Text Books:

1. Design through Verilog HDL – T.R. Padmanabhan and B. Bala Tripura Sundari, WSE, 2004 IEEE press.
2. A Verilog Primer – J. Bhaskar, BSP, 2003.
3. A VHDL Primer - J. Bhaskar, PHI, 3rd edition

Reference Books:

1. Fundamentals of Logic Design with Verilog – Stephen. Brown and Zvonko Vranesic, TMH, 2005.
2. Digital Systems Design using VHDL – Charles H Roth, Jr. Thomson Publications, 2004.
3. Advanced Digital Design with Verilog HDL – Michael D. Ciletti, PHI, 2005.

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – I Sem.

DIGITAL SIGNAL AND IMAGE PROCESSING

Subject Code: 22MVL1002

L	T	P	C
3	0	0	3

Course Objectives:

- Thorough understanding of frequency domain analysis of discrete time signals
- Ability to design & analyze DSP systems like FIR and IIR Filter etc
- The fundamentals of digital image processing
- Understand Image enhancement, restoration compression techniques used in digital image processing
- Understand Color Image processing with different planes
- Design and implement algorithms that perform basic image processing

Course Outcomes:

At the end of this course, students will be able to

CO 1. Analyze discrete-time signals and systems in various domains
CO 2. Design and implement filters using fixed point arithmetic targeted for embedded platforms
CO 3. Compare algorithmic and computational complexities in processing and coding digital images.
CO 4. Learn different techniques employed for the enhancement and Compression of images.
CO 5. Analyze Color Image processing with different planes
CO 6. Analyze various Image Processing algorithms

UNIT-I:

Review of Discrete Time signals and systems, Characterization in time and Z and Fourier – Domain, Fast Fourier Transform algorithms – In-place computations, Butterfly computations, bit Reversal's.

UNIT-II:

Digital Filter design: FIR - Windowing and Frequency Sampling, IIR – Impulse Invariance, bilinear Transformation.

UNIT-III:

Fixed point implementation of filters – challenges and techniques.

UNIT- IV:

Digital Image Acquisition, Enhancement, Restoration, Digital Image Coding and Compression – JPEG and JPEG 2000.

UNIT-V:

Color Image processing – Handling multiple planes, computational challenges.

UNIT-VI:

VLSI architectures for implementation of Image Processing algorithms, Pipelining.

Text Books:

1. J.G. Proakis, Manolakis "Digital Signal Processing", Pearson, 4th Edition
2. Gonzalez and Woods, "Digital Image Processing", PHI, 3rd Edition
3. S. K. Mitra. "Digital Signal Processing – A Computer based Approach", TMH, 3rd Edition, 2006

Reference Books:

1. A. K. Jain, "Fundamentals of Digital Image Processing", Prentice Hall
2. KeshabParhi, "VLSI Digital Signal Processing Systems – Design and Implementation",

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – I Sem.

VLSI TECHNOLOGY & DESIGN
(Elective - I)

Subject Code: 22MVL1003

L	T	P	C
3	0	0	3

Course Objectives:

- The main objective of this course is to introduce basic concepts of microelectronics, layout designing, floor planning and algorithms used in the chip designing process.

Course Outcomes:

CO 1. Student is able to understand the concepts of and electrical properties of MOS technologies.
CO 2. Student is able to understand different types layout designing tools and floor planning methods used in chip design.
CO 3. Student is able to design combinational logic networks and sequential systems.
CO 4. Student is able to understand CAD algorithms used in chip design.

UNIT – I:

REVIEW OF MICROELECTRONICS AND INTRODUCTION TO MOS TECHNOLOGIES: (MOS, CMOS, Bi CMOS) Technology trends and projections. Lithography, Oxidation, Ion implantation, Metalization and Diffusion techniques.

BASIC ELECTRICAL PROPERTIES OF MOS, CMOS & BICOMS CIRCUITS: Ids-Vds relationships, Threshold voltage Vt, Gm, Gds and Wo, Pass Transistor, MOS,CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT – II:

LAYOUT DESIGN AND TOOLS: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools. LOGIC GATES & LAYOUTS: Static complementary gates, switch logic, Alternative gate circuits, low power gates, Resistive and Inductive interconnect delays.

UNIT – III:

COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, interconnect design, power optimization, Switch logic networks, Gate and Network testing.

UNIT – IV:

SEQUENTIAL SYSTEMS: Memory cells and Arrays, clocking disciplines, System Design, power optimization, Design validation and testing.

UNIT – V:

FLOOR PLANNING & ARCHITECTURE DESIGN: Floor planning methods, off-chip connections, High-level synthesis, Architecture for low power, SOCs and Embedded CPUs, Architecture testing.

UNIT – VI:

INTRODUCTION TO CAD SYSTEMS (ALGORITHMS) AND CHIP DESIGN: Layout Synthesis and Analysis, Scheduling and printing, Hardware/Software Co-design, chip design methodologies-A simple Design example.

Text Books:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian et. al (3 authors) PHI of India Ltd.,2005.
2. Modern VLSI Design, 3rd Edition, Wayne Wolf, Pearson Education, 5th Indian Reprint, 2005.

Reference Books:

1. Principals of CMOS Design – N.H.E Weste, K.Eshraghian, Adison Wesley, 2nd Edition.
2. Introduction to VLSI Design – Fabricius, MGH International Edition, 1990.
3. CMOS Circuit Design, Layout and Simulation – Baker, Li Boyce, PHI, 2004.
4. VLSI Technology - 2nd Edn..- S.M.Sze.

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – I Sem.

CMOS ANALOG IC DESIGN
(Elective - I)

Subject Code: 22MVL1004

L	T	P	C
3	0	0	3

Course Objectives:

- To provide theoretical basics for analysis and design of analog integrated circuits.
- To understand various current mirror configurations in application to different amplifiers.
- To understand various advanced current mirror configurations and comparators.
- To introduce PLL concept in integrated circuits.
- To understand switched capacitor circuits for realizing analog signal processing in MOS integrated circuits.
- To introduce Nyquist data converters useful in many applications.

Course Outcomes:

CO 1. Design two stage CMOS operational amplifiers and compensation techniques.
CO 2. Illustrate current mirror circuits in single stage CMOS operational amplifiers.
CO 3. Illustrate advanced current mirrors and comparators.
CO 4. Understand PLL use in integrated circuits
CO 5. Understand switched capacitor circuits.
CO 6. Design and analyze CMOS A/D and D/A data converters of different types.

UNIT – I:

BASIC OPERATIONAL AMPLIFIER DESIGN AND COMPENSATION: General considerations one – state op-amps, Two Stage CMOS Operational Amplifier, opamp gain, frequency response, slew rate, systematic offset voltage, Feedback and Operational Amplifier Compensation-linear settling time, opamp compensation, compensating the two stage opamp, lead compensation, compensation independent of process and temperature.

UNIT – II:

CURRENT MIRRORS AND SINGLE STAGE AMPLIFIERS: Simple COMS, BJT current mirror, Cascode Wilson Wilder current mirrors. Common Source amplifier source follower, common gate amplifier

NOISE: Types of Noise – Thermal Noise-flicker noise- Noise in opamps- Noise in common source stage noise band width.

UNIT – III:

ADVANCED CURRENT MIRRORS & COMPARATORS: Advanced Current Mirrors, Folded-Cascode Operational Amplifier, Current Mirror Operational Amplifier, Linear settling time revisited, Fully Differential Operational Amplifier. Common Mode Feedback Circuits, Current Feedback Operational Amplifier.

UNIT – IV:

PHASED LOCKED LOOP DESIGN: PLL concepts- The phase locked loop in the locked condition Integrated circuit PLLs– phase Detector- Voltage controlled oscillator case study: Analysis of the 560 B Monolithic PLL.

UNIT – V:

SWITHCHED CAPACITORS CIRCUITS: Basic Building blocks op-amps capacitors switches – non-over lapping clocks-Basic operations and analysis-resistor equivalence of la switched capacitor-parasitic sensitive integrator parasitic insensitive integrators signal flow graph analysis- First order filters- switch sharing fully differential filters – charged injections-switched capacitor gain circuits parallel resistor –capacitor circuit – preset table gain circuit –other switched capacitor circuits – full wave rectifier – peak detector sinusoidal oscillator.

UNIT – VI:

COMPARATORS: Using an op-amp for comparator-charge injection errors- latched comparator.
NYQUIST RATE D/A CONVERTERS: Decoder based converter resistor storing converters folded resister string converter –Binary scale converters – Binary weighted resistor converters – Reduced resistance ratio ladders – R-2R based converters – Thermometer code current mode D/A converters.
NYQUIST RATE A/D CONVERTERS: Integrating converters – successive approximation converters. DAC based successive approximation – flash converters time interleaved A/D converters.

Text Books:

1. Analog Integrated circuit Design by David A Johns, Ken Martin, John Wiley & Sons.
2. Analysis and design of Analog Integrated Circuits, by Gray, Hurst Lewis, Meyer. John Wiley & Sons.

Reference Books:

1. Design of Analog CMOS Integrated Circuits, Behzad Razavi, TMH
2. Gregolian & Temes, “Analog MOS Integrated Circuits”, John Wiley, 1986.

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – I Sem.

DSP PROCESSORS AND ARCHITECTURE
(Elective - I)

Subject Code: 22MVL1005

L	T	P	C
3	0	0	3

Course Objectives:

- To have an overview of digital signal processing.
- To understand the design of various building blocks of DSP processors.
- To understand architecture and programming of DSP processors,
- To design of real-time DSP systems
- Analyze the Implementation of DSP algorithms using both the fixed-point and floating-point processors.
- To understand the designing of programmable DSP processors.

Course Outcomes:

At the end of the course, the student will be able to:

CO 1. Understand required building blocks to design a DSP processors.
CO 2. Understand different DSP processors and basic programming skills.
CO 3. Learn basic architectural features that programmable DSP devices should have, their operations & their computational accuracies in DSP implementation.
CO 4. Analyze DSP processors TMS 320C 54XX for implementation of DSP algorithms
CO 5. Analyze interfacing techniques with various I/O peripherals.
CO 6. Understand Interfacing Memory and I/O Peripherals to Programmable DSP Devices

UNIT – I:

INTRODUCTION TO DIGITAL SIGNAL PROCESING: Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation.

UNIT – II:

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT – III:

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

EXECUTION CONTROL AND PIPELINING: Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT – IV:

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS: Commercial Digital signal- processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT – V:

IMPLEMENTATIONS OF BASIC DSP AND FFT ALGORITHMS: The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

UNIT – VI:

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

Text Books:

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. S. Chand & Co, 2000.

Reference Books:

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkata Ramani and M. Bhaskar, TMH, 2004.
2. Digital Signal Processing – Jonatham Stein, John Wiley, 2005

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – I Sem.

VLSI SIGNAL PROCESSING
(Elective - II)

Subject Code: 22MVL1006

L	T	P	C
3	0	0	3

Course Objectives:

- Understand the pipelining and parallel processing techniques to the VLSI system
- Analyze the retiming, unfolding & folding concepts for register minimization
- Understand the systolic architectures
- Understand the various arithmetic circuits for signal processing
- Understand and apply the fast convolution algorithms for signal processing applications
- Explain different low power algorithms.
- Explain redundant number representation and numerical strength reduction algorithms.

Course Outcomes:

At the end of this course, students will be able to

CO 1. Design parallel processors in VLSI systems
CO 2. Implement the register minimization using the retiming, unfolding & folding concepts.
CO 3. Design systolic architecture using canonical mapping and generalized mapping.
CO 4. Analyze the fast convolution algorithms and use them for signal processing applications
CO 5. Design low power multipliers using bit level arithmetic circuits.
CO 6. Design low power multipliers using multiple constant algorithms.

UNIT – I:

INTRODUCTION TO DSP :Introduction, Typical DSP algorithms, Representation of DSP algorithms , Iteration Bound-Data flow graph Representation, loop bound, iteration bound, algorithms for computing iteration bound, iteration bound of multirate dataflow graphs. Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power,

UNIT – II:

RETIMING: Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques

UNFOLDING: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding

FOLDING: Introduction - Folding Transform – Register minimization Techniques – Register minimization in folded architectures – folding of multirate systems

UNIT – III:

SYSTOLIC ARCHITECTURE DESIGN: Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain delays.

UNIT – IV:

FAST CONVOLUTION: Introduction – Cook-Toom Algorithm – Winograd algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

ALGORITHM STRENGTH REDUCTION FILTERS AND TRANSFORMS: Introduction, parallel FIR filters, Discrete cosine Transform and Inverse DCT

UNIT – V:

BIT-LEVEL ARITHMETIC ARCHITECTURES-Introduction, parallel multipliers, Interleaved floor plan and Bit plane based digital filters, Bit-Serial Multipliers, Bit-Serial filter design and implementation, Canonic Signed Digit Arithmetic, Distributed Arithmetic.

UNIT – VI:

REDUNDANT ARITHMETIC: Introduction, Redundant number representation, Carry free Radix- 2 Addition and Subtraction, Hybrid Radix-4 addition, Radix -2 Hybrid redundant multiplication architectures, data format conversion, redundant to non redundant converter

NUMERICAL SRENGTH REDUCTION: Introduction, Sub expression Elimination, Multiple constant multiplications, Sub expression sharing in digital filters, additive and multiplicative number splitting.

Text Books:

1. Keshab K. Parthi, VLSI Digital Signal Processing- System Design and Implementation –1998, Wiley Inter Science.
2. Kung S. Y, H. J. While House, T. Kailath, VLSI and Modern Signal processing, 1985, Prentice Hall.

Reference Books:

1. Jose E. France, Yannis Tsividis, Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing –1994, Prentice Hall.
2. Medisetti V. K, VLSI Digital Signal Processing, IEEE Press (NY), USA, 1995.

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – I Sem.

DIGITAL SYSTEM DESIGN
(Elective - II)

Subject Code: 22MVL1007

L	T	P	C
3	0	0	3

Course Objectives:
The main objective of this course is to
- Explain the designing principles of various digital systems
- Analyze a given digital system and decompose it into logical blocks involving both combinational and sequential circuit elements.
- Explain Reduction of state tables and state assignments.
- Describe the Fault Modeling and Test pattern Generation methods.
- Describe PLA minimization and testing.
- Describe an asynchronous sequential machines

Course Outcomes:
Student will be able to
CO 1. Apply knowledge of digital systems, Sequential Circuit Design and design of digital logic circuits
CO 2. Explain fault modeling and classes.
CO 3. Apply knowledge of different algorithms for generating test patterns.
CO 4. Detect states and faults in sequential circuits.
CO 5. Explain PLA minimization and testing.
CO 6. Analyze an asynchronous sequential machines

UNIT – I:
DESIGN OF DIGITAL SYSTEMS: ASM charts, Data path design and Control Logic implementation, Reduction of state tables, State assignments.

UNIT – II:
SEQUENTIAL CIRCUIT DESIGN: Design of Iterative circuits, Design of sequential circuits using ROMs and PLAs, Sequential circuit design using CPLD, FPGAs.

UNIT – III:
FAULT MODELING: Fault classes and models – Stuck at faults, bridging faults, transition and intermittent faults.
TEST GENERATION: Fault diagnosis of Combinational circuits by conventional methods – Path Sensitization technique, Boolean difference method, Kohavi algorithm.

UNIT – IV:
TEST PATTERN GENERATION: D – algorithm, PODEM, Random testing, transition count testing, Signature analysis and testing for bridging faults.
FAULT DIAGNOSIS IN SEQUENTIAL CIRCUITS: State identification, Machine identification, and fault detection experiment.

UNIT – V:
PROGRAMMING LOGIC ARRAYS: Design using PLA's, PLA minimization and PLA folding. PLA TESTING: Fault models, Test generation and Testable PLA design.

UNIT – VI:
ASYNCHRONOUS SEQUENTIAL MACHINE: fundamental mode model, flow table, state reduction, minimal closed covers, races, cycles and hazards.

Text Books:
1. Z. Kohavi – "Switching & finite Automata Theory" (TMH).
2. N. N. Biswas – "Logic Design Theory" (PHI).
3. Nolman Balabanian, Bradley Calson – "Digital Logic Design Principles" – Wily Student Edition 2004.

Reference Books:
1. M. Abramovici, M. A. Breues, A. D. Friedman – "Digital System Testing and Testable Design", Jaico Publications.
2. Charles H. Roth Jr. – "Fundamentals of Logic Design".
3. Frederick. J. Hill & Peterson – "Computer Aided Logic Design" – Wiley 4th Edition.

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M.Tech (VLSI System Design) – I Sem.

EMBEDDED SYSTEMS DESIGN
(Elective – II)

Subject Code: 22MVL1008

L	T	P	C
3	0	0	3

Course Objectives:

- Understand the general overview of Embedded Systems; distinguish between ES and GPCS, components & major application areas of ES.
- Learn about Characteristics and Quality attributes of Embedded Systems and core of the embedded system.
- Gain the ability to make intelligent choices for selection of memory and different communication interfaces.
- Understand different embedded firmware design approaches and languages.
- Study the overview of Real Time Operating Systems
- To clearly differentiate the different issues that arises in real time operating systems.

Course Outcomes:

CO 1. Distinguish Embedded System & General Purpose Computing System and formulate the typical embedded system
CO 2. Describe the characteristics, Quality Attributes of an Embedded System and core of the embedded systems.
CO 3. Explain the concepts of different types of memory and communication interfaces.
CO 4. Use firmware approaches and modern engineering tools necessary for developing firmware & hardware in embedded system design
CO 5. Explain the concepts of Real Time Operating System (RTOS) based embedded system design.
CO 6. Identify the issues in real time operating systems and choose an appropriate RTOS.

UNIT -I:
Introduction to Embedded Systems Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems,

UNIT -II:
Characteristics and Quality Attributes of Embedded Systems. Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS),

UNIT-III:
Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT -IV:
Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer. Embedded Firmware: Embedded Firmware Design Approaches and Development Languages.

UNIT -V:
RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT -VI:
Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

Text Books:
1. Introduction to Embedded Systems - Shibu K.V, McGraw Hill.

Reference Books:
1. Embedded Systems - Raj Kamal, TMH.
2. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.
3. Embedded Systems – Lyla, Pearson, 2013
4. An Embedded Software Primer - David E. Simon, Pearson Education.

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – I Sem.

HDL PROGRAMMING LAB

Subject Code: 22MVL1101

L	T	P	C
0	0	4	2

Course Objectives:

- Study the Xilinx software.
- Analyze and experience with principle of designing digital circuits
- Simulate the digital circuits by using VHDL/Verilog.
- Synthesize the digital circuits by using VHDL
- Implement the digital circuits by using VHDL.
- Implement Digital Circuits using FPGA and CPLD devices.

Course Outcomes:

CO 1. Simulate the digital circuits by using VHDL/ Verilog.
CO 2. Synthesis and implement the digital circuits by using VHDL.
CO 3. Generate RTL schematics and timing constraints.
CO 4. Produce power report and Place and Route report of digital circuit synthesis.
CO 5. Implement the digital circuits by using FPGA devices
CO 6. Design Digital Circuits using FPGA and CPLD devices.

The students are required to simulate, synthesize and implement the following experimental part, on the VHDL/Verilog environment.

1. Digital Circuits Description using Verilog / VHDL
2. Verification of the Functionality of Designed circuits using function Simulator.
3. Timing simulation for critical path time calculation.
4. Synthesis of Digital circuits
5. Place and Route techniques for major FPGA vendors such as Xilinx, Altera and Actel etc.
6. Implementation of Designed Digital Circuits using FPGA / CPLD devices

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – I Sem.

DIGITAL SIGNAL AND IMAGE PROCESSING LAB

Subject Code: 22MVL1102

L	T	P	C
0	0	4	2

Course Objectives::

- Understand the basic digital signal, image and video processing algorithms and their implementation in C or MATLAB.

Course Outcomes::

CO 1. Understand the fundamentals of image and video signal processing and associated techniques.
CO 2. Understand how to solve practical problems with some basic image and video signal processing techniques.
CO 3. Have the ability to design simple systems for realizing some multimedia applications with some basic image and video signal processing techniques.

The students are required to simulate the following experimental parts on the MATLAB environment by consider the relevant application based examples.

PART-1: Digital Signal Processing

1. Discrete-time Signals and Systems in the time domain.
2. z-Transforms and inverse z-Transforms.
3. The Discrete Fourier Transform properties.
4. FIR Filter Design.
5. IIR Filter Design.
6. Applications in Adaptive Filtering.

PART-2: Image Processing

1. Image Enhancement in Spatial Domain
2. Fourier Transform of an Image
3. Enhancement in Frequency Domain.
4. Image segmentation
5. Image Compression.

PART-3: Video Processing

1. Divide 1sec video into frames
2. Filter operations on video(Smoothing and Sharpening)
3. Motion estimate of an object in a video.

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – I Sem.

RESEARCH METHODOLOGY AND IPR

Subject Code: 22MCC1001

L	T	P	C
2	0	0	2

Course Objectives:

Course Outcomes:

At the end of this course, students will be able to

CO 1. Understand research problem formulation
CO 2. Analyze research related information Follow research ethics
CO 3. Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
CO 4. Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
CO 5. Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D,
CO 6. Understand creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT-I:
Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and Course Objectives: of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT-II:
Effective literature studies approaches, analysis Plagiarism, Research ethics,

UNIT III:
Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee

UNIT -IV:
Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT-V:
Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

UNIT-VI:

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

Text Books:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science& engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
3. Ranjit Kumar, 2nd Edition , "Research Methodology: A Step by Step Guide for beginners"
4. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
5. Mayall , "Industrial Design", McGraw Hill, 1992.
6. Niebel , "Product Design", McGraw Hill, 1974.

Reference Books:

1. Asimov , "Introduction to Design", Prentice Hall, 1962.
2. Robert P. Merges, Peter S. Menell, Mark A. Lemley, " Intellectual Property in New Technological Age", 2016.
3. T. Ramappa, "Intellectual Property Rights Under WTO", S. Chand, 2008

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – I Sem.
ENGLISH FOR RESEARCH PAPER WRITING
(Audit Course)

Subject Code: 22MAC1001

L	T	P	C
2	0	0	0

Course Outcomes:

At the end of this course, students will be able to

CO 1. Students will be able to write paper with clarity and brevity
CO 2. Students will be able to interpret their findings in their own way unaffected by external factors
CO 3. Students will be able to get accurate results with an astute understanding of the subject
CO 4. Students will be able to begin paper writing more aptly
CO 5. Students will be able to write methods, results, discussions and conclusion in their paper more logically
CO 6. Students will be able to use phrases competently to express their ideas

UNIT–I:

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT–II:

Clarifying Who Did What, Highlighting Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction

UNIT–III:

Review of the Literature, Methods, Results, Discussion, Conclusions, Final Check

UNIT–IV:

Key skills needed when writing a Title, an Abstract, an Introduction and a Review of the Literature

UNIT–V:

Skills needed when writing Methods, Results, Discussions and Conclusion

UNIT-VI:

Useful phrases, how to ensure paper is as good as it could possibly be the first- time Submission

Text Books:

1. Goldbort R (2006). *Writing for Science*. Yale University Press.
2. Day R (2006). *How to Write and Publish a Scientific Paper*. Cambridge University Press.

Reference Books:

1. Highman N (1998). *Handbook of Writing for the Mathematical Sciences*, SIAM. Highman's book .
2. Adrian Wallwork . *English for Writing Research Papers*. Springer New York Dordrecht Heidelberg London, 2011.

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – I Sem.

DISASTER MANAGEMENT
(Audit Course)

Subject Code: 22MAC1002

L	T	P	C
2	0	0	0

Course Outcomes:

At the end of the course the student will be able to:

CO 1. Know the Disaster Concepts to Management.
CO 2. Ability to Categorize Disasters & Preparedness plans for disaster response.
CO 3. Ability to analyze seismic vulnerable location in various parts of India
CO 4. Monitoring and evaluation plan for disaster response, setting up of early warning systems for risk reductions
CO 5. Ability to analyze seismic vulnerable location in various parts of India
CO 6. Analyze the statistical approach on land slides

UNIT-I:

Concept of Disaster Management. Types of Disasters. Disaster mitigating agencies and their organizational structure at different levels

UNIT-II:

Overview of Disaster situations in India: Vulnerability profile of India and vulnerability mapping including disaster – prone areas, communities, places.

UNIT-III:

Disaster preparedness – ways and means; skills and strategies; rescue, relief, reconstruction and rehabilitation.

UNIT-IV:

Case studies: Lessons and experiences from various important disasters in India.

UNIT-V:

Seismic vulnerability of urban areas.: Seismic response of R.C. frame buildings with soft first storey. Preparedness for natural disasters in urban areas. Sulbh technology for sanitation improvement in urban habitat. Landslide hazards zonation mapping and geo-environmental problems associated with the occurrence of landslides.

UNIT-VI:

Statistical approach to study landslides: Landslide casual factors in urban areas. Roads and landslide hazards in Himalayas. Lateral strength of masonry walls. A numerical model for post earthquake fire response of structures. Cyclone resistant house for coastal areas. Disaster resistant construction role of insurance sector. Response of buried steel pipelines carrying water subjected to earthquake ground motion. Preparedness and planning for an urban earthquake disaster. Urban settlements and natural hazards. Role of knowledge based expert systems in hazard scenario.

Text Book:

1. Natural Hazards in the Urban Habitat" by Iyengar, C.B.R.I., Tata McGraw Hill.
2. Natural Disaster management", Jon Ingleton(Ed), Tulor Rose

Reference Books:

1. Disaster Management", R.B. Singh (Ed), Rawat Publications,2006
2. Anthropology of Disaster management", Sachindra Narayan, Gyan Publishing House,2000

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – I Sem.

CONSTITUTION OF INDIA
(Audit Course)

Subject Code: 22MAC1003

L	T	P	C
2	0	0	0

Course Outcomes:

By the end of this course the student will be able to:

CO 1. Realize the rigidness of our Indian Politics and Administrative aspects.
CO 2. A Student can understand our nation federalism.
CO 3. Can assess different types of risks involved in misadministration.
CO 4. Can create competitive advantage.
CO 5. Summarizes the legal, Administrative, Political and Financial aspects for betterment of the National building.
CO 6. To assess the growth of Indian opinion regarding modern Indian intellectuals' Constitutional role and entitlement to civil and economic rights as well as the emergence of nationhood in the early years of Indian nationalism

UNIT – I:

Introduction: Historical perspective of the constitution of India - Salient features of The Indian Constitution –Features: Fundamental Rights (Article 12 to 35), Duties (51 A – 1976 emergency) and Directive principles (Article 36 to 51) of State Policy - Articles 14 to 18- Articles 19 - Article 21

UNIT-II:

Amendment Procedure of The Indian Constitution: 42^{nd} amendment (Mini Constitution) - 44^{th}amendment (1978 – Janatha Govt.)

UNIT – III:

Local Administration: District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of ElectedRepresentative, CEO of Municipal Corporation, Pachayati raj: Introduction, PRI: ZilaPachayat, Elected officials andtheir roles, CEO ZilaPachayat: Position and role, Block level: Organizational Hierarchy (Different departments),Village level: Role of Elected and Appointed officials, Importance of grass root democracy

UNIT – IV:

Parliamentary form of Govt. In India: President of India - Emergency provisions -National Emergency – Article 352 President Rules – Article 356 - Financial Emergency – Article 360Prime Minister and Cabinet - Supreme Court of India (Indian Judiciary)

UNIT – V:

Indian Federalism: Union – State relations; - Legislative, Administrative and Financial relations. LokSabha, RajyaSabha, VidhanSabha & VidhanParishad - Composition; Speaker, Chairman, Privileges, Legislative procedure.

UNIT – VI:

Parliamentary Committees: Public Accounts Committee - Estimates Committee - Committee on Public Undertakings. - Election commission of India (Article -324) - Comptrollar and Auditor General (CAG) of India (Article – 148 to 150) - Finance Commission (Article – 280) - NeethiAayog (Planning Commission) and - Political Parties.

Text Books:

1. D.D Basu – Indian Constitution.
2. Dr. D. Surannaidu – Indian Political System.
3. Madhav Khosla – The Indian Constitution.

Reference Books:

1. The Constitution of India, 1950 (Bare Act), Government Publication.
2. M. P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis, 2014.

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – I Sem.

PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS
(Audit Course)

Subject Code: 22MAC1004

L	T	P	C
2	0	0	0

Course Outcomes:

By the end of this course the student will be able to:

CO 1. Realize that everyone is responsible for creating his/her own personality.
CO 2. Gain knowledge of the importance of developing virtues like wisdom and courage and knowing what are good acts (do's) and bad acts (don'ts).
CO 3. Understand the key message of Bhagavad Gita which is experiencing spiritual oneness by practicing any or all of the karma, bhakti, dhyana or raja, and jnana yogas.
CO 4. Know the vedantic perspective of lifewith regards to understanding human nature, art of living and technique of self-unfoldment.
CO 5. Realize the goal and means to attain self-realization which is the only way to attain liberation.
CO 6. Become aware that sub-conscious mind which is full of desires is the main obstacle for self-realization and spiritual practices help in eliminating these desires.

UNIT-I:

Personality Development: It is Personality that Matters – Laws of Personality Development – Different Layers of Personality – Pleasure is not the Goal – How to Change Our Character – Control Your Negative Emotions – Change Yourself First – Take Whole Responsibility of Yourself.

UNIT-II:

Holistic Personality Development: (from BhartruhariNeetiSatakam) Wisdom (Verses 19, 20, 21, 22) – Pride & Heroism (Verses 29, 31, 32) – Virtues (Verses 26, 28, 63, 65) – Don'ts (Verses 52, 53, 59) – Do's (Verses 71, 73, 75, 78)

UNIT-III:

Bhagavad Gita:

Chapter 2 – Verses 17, 56, 62, 68
Chapter 3 – Verses 13, 21, 27, 35, 36, 37, 42
Chapter 4 – Verses 18, 38, 39
Chapter 6 – Verses 5, 13, 17, 23, 35
Chapter 12 – Verses 13, 14, 15, 16, 17, 18
Chapter 18 – Verses 37, 38, 45, 46, 48, 63

UNIT-IV:

Vedantic Perspective of Life: Brief discussion of major topics in Understanding Human Nature – Art of Living – Technique of Self Unfoldment

UNIT-V

Vivekachudamani: Self-realization is the means of liberation – Means to Self-realization – Qualifications of a Spiritual Aspirant – 4-fold Spiritual Discipline

UNIT-VI:

Mind and Its Mysteries: What is Mind? Mind and body, Mind and food – Mental faculties – Theory of perception, Memory, Imagination, Thought-Culture, Desires – Cultivation of Virtues, Control of Senses and Mind – Concentration, Meditation and Enlightenment.

Text Books:

1. Personality Development, Swami Vivekananda, Advaita Ashrama Publication, ISBN 978817552246
2. Three Satakam of Bharatrhari (Niti, Srngara, Vairagya), P. Gopinath, Rashtriya Sanskrit SansthanPubllication.
3. Bhagavad Gita, Swami Swarupananda, Advaita Ashram Publication.
4. Vedanta – Science of Life, 3 Vols, Swami Chinmayananda, Chinmaya Mission Pub
5. (Vol1 – Understanding Human Nature, Vol2 – Art of Living, Vol3 – Technique of Self-Unfoldment)
6. Message of Vivekachudamani, Swami Ranganadhananda, Advaita Ashrama Publication, ISBN 817553089
7. Mind, Its Mysteries and Control, Swami Sivananda, Divine Life Society Publication.

Reference Books:

1. https://archive.org/download/satakasofbhartri00bharuoft/satakasofbhartri00bharuoft.pdf
2. Bhagavad Gita – Sadhaka Sanjivani, Swami Ramsukhdas, Gita Press Publication (1080, 1081)
3. The Goal and The Way, Swami Satprakashananda, Ramakrishna Math Publication
4. Spiritual Quest, Swami Tapasyananda, Ramakrishna Math Publications, ISBN 8171204562
5. Mind According to Vedanta, Swami Satprakashanada, Ramakrishna Math Publication, ISBN 8171206506

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – II Sem.

MIXED SIGNAL IC DESIGN

Subject Code : 22MVL1009

L	T	P	C
3	0	0	3

Course Objectives:

- To introduce circuit design concepts for basic building blocks used in mixed signal integrated circuit designs.
- To provide students with the skills to design mixed-signal integrated circuits with these building blocks.
- To Understand the design of circuits in IC form especially both digital and analog designs
- Understand the design of specific circuits like PLL,A/D,D/A
- To Understand over sampling converters starts with Switched Capacitor circuits
- To understanding the circuits by considering so many parameters may arises problems which need to be solve to get optimization

Course Outcomes:

At the end of the course the student will be able to

CO 1. Learn analysis of switched capacitor circuits.
CO 2. Learn non ideal effects in switched capacitor circuits.
CO 3. Know dynamics of PLL blocks.
CO 4. Demonstrate the fundamentals of data converters.
CO 5. Compare different data converters.
CO 6. Learn over sampling converters.

UNIT -I:

Switched Capacitor Circuits: Introduction to Switched Capacitor circuits - basic building blocks, Operation and Analysis.

UNIT –II:

Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, bi-quad filters.

UNIT -III:

Phased Lock Loop (PLL): Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT -IV:

Data Converter Fundamentals: DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT -V:

Nyquist Rate A/D Converters: Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT -VI:

Oversampling Converters: Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

Text Books:

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford UniversityPress, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edition, 2013

Reference Books:

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – II Sem.

DESIGN OF FAULT TOLERANT SYSTEMS

Subject Code: 22MVL1010

L	T	P	C
3	0	0	3

Course Objectives:

- Design systems to achieve goals like dependability, reliability, availability, safety, performability, maintainability, and testability
- Explain about fault tolerant systems
- Understand self checking circuits
- Understand fail safe design
- Analyze testability for combinational and sequential circuits
- Describe LFSR and BIST concepts

Course Outcomes:

At the end of the course the student will be able to

CO 1. Calculate dependability, reliability, availability, safety, performability, maintainability, and testability
CO 2. Analyze redundancy systems
CO 3. Design circuits that generate test patterns
CO 4. Describe fail safe design circuits.
CO 5. Develop the combinational and sequential circuits for testability
CO 6. Summarize the LFSR and built in self test concepts

UNIT – I:

BASIC CONCEPTS: Reliability concepts, Failure & Faults, Reliability and failure rate, Relation between reliability and meantime between failure, Maintainability and Availability, Reliability of series, Parallel and Parallel-Series combinational circuits.

UNIT – II:

FAULT TOLERANT DESIGN: Basic concepts – Static, dynamic, hybrid, Triple Modular Redundant System, Self purging redundancy, Siftout redundancy (SMR), SMR Configuration, Use of error correcting code, Time redundancy and software redundancy.

UNIT – III:

SELF CHECKING CIRCUITS: Basic concepts of Self checking circuits, Design of Totally Self Checking checker, Checkers using m out of n codes, Berger code, Low cost residue code.

UNIT – IV:

FAIL SAFE DESIGN: Strongly fault secure circuits, fail-safe design of sequential circuits using partition theory and Berger code, totally self-checking PLA design.

UNIT – V:

DESIGN FOR TESTABILITY FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS: Basic concepts of testability, controllability and observability, the Reed Muller's expansion technique, OR - AND-OR design, use of control and syndrome testable design. Level Sensitive Scan Design (LSSD).

UNIT – VI:

Theory and operation of LFSR, LFSR as Signature analyzer, Multiple-input Signature Register. BUILT IN SELF TEST: BIST concepts, Test pattern generation for BIST exhaustive testing, pseudorandom testing, pseudo exhaustive testing, constant weight patterns.

Text Books:

1. Parag K. Lala – "Fault Tolerant & Fault Testable Hardware Design" (PHI)
2. M. Abramovili, M.A. Breues, A. D. Friedman – "Digital Systems Testing and Testable Design" Jaico publications.

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – II Sem.

LOW POWER VLSI DESIGN
(Elective-III)

Subject Code: 22MVL1011

L	T	P	C
3	0	0	3

Course Objectives:

- To familiarize with the different types of Low power design methods/models used in VLSI design.
- To study the concepts on different levels of power estimation and optimization techniques.
- Introduce the technology, design concepts, electrical properties and modelling of Very Large Scale Integrated circuits.
- Identify sources of power in an IC and suitable techniques to reduce the power dissipation in ICs
- Design of CMOS low power IC, approaches for power consumption estimation
- To understand methods of reducing switching & leakage power.

Course Outcomes:

At the end of the course the student will be able to

CO 1. Describe in detail the need and use of low power devices in the design of VLSI.
CO 2. Design chips used for battery-powered systems and high-performance circuits not exceeding power limits.
CO 3. Apply in practice technology-level, circuit-level, and system-level power optimization techniques.
CO 4. Design a significant VLSI design project having set of objective criteria and design constraints.
CO 5. Design the conventional CMOS and BICOMS circuits using logic gates.
CO 6. Analyze the quality measures and design perspectives of latches and Flip-Flaps.

UNIT – I:

LOW POWER DESIGN AN OVER VIEW: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

MOS/BiCMOS PROCESSES: Realization of Bi CMOS processes: Low cost-medium speed digital, High performance-High cost digital, Analog/Digital Integrated BiCMOS.

UNIT – II:

ISOLATION IN BiCMOS: Isolation in BiCMOS, Isolation Techniques in MOS - LOCOS, Shallow and Deep Trench, Advanced Isolation techniques - Dielectric Isolation (DI), Wafer bonding, Smart cut process.

LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES: Deep submicron processes - Key process steps , SOI CMOS, lateral BJT on SOI, Future trends and directions of CMOS/BiCMOS processes.

UNIT – III:

DEVICE MODELING: MOSFET Spice Models, Advanced MOSFET models, limitations of MOSFET models, Bipolar models - Ebers Moll model, Gummel poon model, HICUM model

UNIT – IV:
Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment

UNIT – V:
CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS and BiCMOS logic gates, Performance Evaluation.
LOW- VOLTAGE LOW POWER LOGIC CIRCUITS: Operation, Performance and comparative Evaluation of Advanced BiCMOS Digital circuits - Full-Swing Multi drain/Multi collector CBiCMOS, Quasi-CBiCMOS, Feedback type BiCMOS, ESD-free Bi CMOS.

UNIT – VI:
LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

Text Books:
1. CMOS/BiCMOS ULSI low voltage, low power by Yeo Rofail/ Gohl (3 Authors)- Pearson Education Asia 1st Indian reprint,2002

Reference Books:
1. Digital Integrated circuits, J.Rabaey PH. N.J 1996
2. CMOS Digital ICs sung-moKang and yusufleblebici 3rd edition TMH2003 (chapter 11)
3. VLSI DSP systems, Parhi, John Wiley & sons, 2003 (chapter 17)
4. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – II Sem.

CAD OF DIGITAL SYSTEM
(Elective-III)

Subject Code: 22MVL1012

L	T	P	C
3	0	0	3

Course Objectives:

- Explain the various algorithms used to design VLSI in automation.
- Illustrate the various optimization techniques in the process of automation.
- Describe various floor planning methods for layout design.
- Describe various Routing techniques for layout design.
- Discuss various MCM technologies
- Analyze various FPGA technologies

Course Outcomes:

At the end of the course the student will be able to

CO 1. Explain VLSI Design Flow, design automation tools and algorithms
CO 2. Examine various Routing algorithms for layout design.
CO 3. Apply various Routing algorithms for layout design.
CO 4. Explain logic synthesis and verification
CO 5. Apply various Routing algorithms for FPGA.
CO 6. Apply various Routing algorithms for MCM.

UNIT – I :

Introduction to VLSI Methodologies – Design and Fabrication of VLSI Devices, Fabrication, Process and its impact on Design.

UNIT – II :

VLSI design automation tools – Data structures and basic algorithms, graph theory and computational complexity, tractable and intractable problems.

UNIT – III :

General purpose methods for combinational optimization – partitioning, floor planning And pin assignment, placement , routing.

UNIT – IV:

Simulation – logic synthesis, verification, high level Synthesis.

UNIT – V:

PHYSICAL DESIGN AUTOMATION OF FPGA'S: FPGA technologies, Physical Design cycle for FPGA's partitioning and routing for segmented and staggered models.

UNIT – VI:

PHYSICAL DESIGN AUTOMATION OF MCM'S: MCM technologies, MCM physical design cycle, Partitioning, Placement – Chip array based and full custom approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, outing and programmable MCM's

Text Book:

1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation".

Reference Books:

1. S.H. Gerez, "Algorithms for VLSI Design Automation.

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – II Sem.

MEMORY TECHNOLOGIES
(Elective-III)

Subject Code: 22MVL1013

L	T	P	C
3	0	0	3

Course Objectives:

- Understand architecture and design semiconductor memory circuits and subsystems.
- Understand various types of Non-Volatile Memories
- Learn various fault models, modes and mechanisms in semiconductor memories and their testing procedures.
- Describe the Semiconductor Memory Reliability and Radiation Effects
- Describe how of the state-of-the-art memory chip design
- Describe various Memory devices

Course Outcomes:

At the end of the course, students will be able to:

CO 1. Select architecture and design semiconductor memory circuits and subsystems.
CO 2. Understand various types of Non-Volatile Memories
CO 3. Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures.
CO 4. Analyze the Semiconductor Memory Reliability and Radiation Effects
CO 5. Know how of the state-of-the-art memory chip design
CO 6. Analyze various Memory devices

UNIT – I :

Random Access Memory Technologies:
Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

UNIT – II :

DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs.SRAM and DRAM Memory controllers.

UNIT – III :

Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

UNIT – IV :

Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.

UNIT – V:

Advanced Memory Technologies and High-density Memory Packing Technologies:
Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices.

UNIT – VI :

Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging

Text Books:

1.Ashok K Sharma, "Advanced Semiconductor Memories: Architectures, Designs and Applications", Wiley Interscience
2. Kiyoo Itoh, "VLSI memory chip design", Springer International Edition

Reference Books:

1. Ashok K Sharma," Semiconductor Memories: Technology, Testing and Reliability , PHI

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – II Sem.

ALGORITHMS FOR VLSI DESIGN AUTOMATION
(Elective-IV)

Subject Code: 22MVL1014

L	T	P	C
3	0	0	3

Course Objectives:

- Explain the various algorithms used to design VLSI in automation.
- Illustrate the various optimization techniques in the process of automation.
- Describe various floor planning methods for layout design.
- Describe various Routing techniques for layout design.
- Discuss various MCM technology
- Discuss various FPGA technology

Course Outcomes:

CO 1. Explain VLSI Design Flow, design automachine tools and algorithms
CO 2. Examine various Routing algorithms for layout design.
CO 3. Apply various Routing algorithms for layout design.
CO 4. Explain logic synthesis and verification
CO 5. Apply various Routing algorithms for FPGA.
CO 6. Apply various Routing algorithms for MCM.

UNIT – I:

PRELIMINARIES: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational Complexity, Tractable and Intractable Problems.

UNIT – II:

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT – III:

Layout Compaction, Placement, Floor planning and Routing Problems, Concepts and Algorithms
MODELING AND SIMULATION: Gate Level Modeling and Simulation, Switch level Modeling and simulation.

UNIT – IV:

LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology, Binary – Decision diagram, Two – Level Logic Synthesis.
HIGH LEVEL SYNTHESIS: Hardware Models, Internal representation of the input algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aqspects of Assignment problem, High – level Transformations.

UNIT – V:

PHYSICAL DESIGN AUTOMATION OF FPGA'S: FPGA technologies, Physical Design cycle for FPGA's partitioning and Routing for segmented and staggered models.

UNIT – VI:

PHYSICAL DESIGN AUTOMATION OF MCM'S: MCM technologies, MCM physical design cycle, Partitioning, Placement – Chip array based and full custom approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, routing and programmable MCM's

TEXT BOOKS:

1. Algorithms for VLSI Design Automation, S.H.Gerez, WILEY student edition, John wiley & Sons (Asia) Pvt.Ltd. 1999.
2. Algorithms for VLSI Physical Design Automation, 3rd edition, Naveed Sherwani,
3. Springer International Edition, 2005

REFERENCE BOOKS:

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, Wiley, 1993
2. Modern VLSI Design: Systems on silicon – Wavne Wolf, Pearson Education Asia, 2nd Edition, 1998

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – II Sem.

CPLD AND FPGA ARCHITECTURE AND APPLICATIONS
(Elective-IV)

Subject Code: 22MVL1015

L	T	P	C
3	0	0	3

Course Objectives:

- Understand the features, architectures & applications of CPLD and FPGA devices.
- Explain the designing methods of CPLD and FPGA devices.
- Describe the architecture of the Altera MAX 7000 family of CPLDs
- Describe the architecture of the Xilinx Virtex FPGA family
- Learn Field programmable gate arrays and realization techniques.
- Discuss different case studies using one hot design methods.

Course Outcomes:

At the end of the course, the student will be able to:

CO 1. List the features and know the architecture of different PLDs
CO 2. Design the different families of CPLD & FPGs
CO 3. Realize out finite state machines
CO 4. Analyze e the architecture of the Xilinx Virtex FPGA family
CO 5. Examine the concept system level design by using design methods
CO 6. Analyze different case studies using one hot design methods.

UNIT –I:

PROGRAMMABLE LOGIC DEVICES: ROM, PLA, PAL, CPLD, FPGA – Features, rchitectures, Programming, Applications and Implementation of MSI circuits using Programmable logic Devices.

UNIT – II:

CPLDs: Complex Programmable Logic Devices, Altera series – Max 5000/7000 series and Altera FLEX logic-10000 series CPLD, AMD's- CPLD (Mach 1 to 5), Cypress FLASH 370 Device technology, Lattice pLSI's architectures – 3000 series – Speed performance and in system programmability.

UNIT – III:

FPGAs: Field Programmable Gate Arrays- Logic blocks, routing architecture, design flow, technology mapping for FPGAs, Case studies Xilinx XC4000 & ALTERA's FLEX 8000/10000, FPGAs: AT &T ORCA's

UNIT – IV:

FINITE STATE MACHINES (FSM): Top Down Design, State Transition Table, State assignments for FPGAs, Realization of state machine charts using PAL, Alternative realization for state machine charts using microprogramming, linked state machine, encoded state machine.

FSM ARCHITECTURES: Architectures Centered around non registered PLDs, Design of state machines centered around shift registers, One Hot state machine, Petrinets for state machines-Basic concepts and properties, Finite State Machine-Case study.

UNIT – V:

DESIGN METHODS: One –hot design method, Use of ASMs in one-hot design method, Applications of one hot design method, Extended Petri-nets for parallel controllers, Meta Stability, Synchronization, Complex design using shift registers.

UNIT – VI:

SYSTEM LEVEL DESIGN: Controller, data path designing, Functional partition, Digital front end digital design tools for FPGAs & ASICs, System level design using mentor graphics EDA tool(FPGA Advantage), Design flow using CPLDs and FPGAs.

CASE STUDIES: Design considerations using CPLDs and FPGAs of parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers.

Text Books:

1. Field Programmable Gate Array Technology - S. Trimberger, Edr, 1994, Kluwer Academic Publications.
2. Engineering Digital Design - RICHARD F.TINDER, 2nd Edition, Academic press.
3. Fundamentals of logic design-Charles H. Roth, 4th Edition Jaico Publishing House.

Reference Books:

1. Digital Design Using Field Programmable Gate Array, P.K.Chan& S. Mourad,1994, Prentice Hall.
2. Field programmable gate array, S. Brown, R.J.Francis, J.Rose ,Z.G.Vranesic, 2007,BSP.

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – II Sem.

COMMUNICATION BUSES AND INTERFACES
(Elective-IV)

Subject Code: 22MVL1016

L	T	P	C
3	0	0	3

Course Objectives:

- Learn different types o**f** Serial Busses and its features
- Understand the Architecture, Data transmission, Layers, Frame formats of CAN
- Explain APIs for configuration, reading and writing data onto serial bus.
- Describe and develop peripherals that can be interfaced to desired serial bus.
- Describe various PCI protocols & applications
- Understand the Serial Communication Protocols

Course Outcomes:

At the end of the course, students will be able to:

CO 1. Select a particular serial bus suitable for a particular application.
CO 2. Describe Architecture, Data transmission, Layers, Frame formats of CAN
CO 3. Develop APIs for configuration, reading and writing data onto serial bus.
CO 4. Design and develop peripherals that can be interfaced to desired serial bus.
CO 5. Analyze Data Streaming Serial Communication Protocol
CO 6. Analyze various PCI protocols & applications

UNIT – I:

Serial Busses- Physical interface, Data and Control signals, features

UNIT – II:

limitations and applications of RS232, RS485, I2C, SPI

UNIT – III:

CAN - Architecture, Data transmission, Layers, Frame formats, applications

UNIT – IV:

PCIe - Revisions, Configuration space, Hardware protocols, applications

UNIT – V:

USB - Transfer types, enumeration, Descriptor types and contents, Device driver

UNIT – VI:

Data Streaming Serial Communication Protocol- Serial Front Panel Data Port (SFPDP) using fibre optic and copper cable

Text Books:

1. Jan Axelson, “Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for
2. Embedded Systems ”, Lakeview Research, 2nd Edition
3. Jan Axelson, “USB Complete”, Penram Publications
4. Mike Jackson, Ravi Budruk, “PCI Express Technology”, Mindshare Press

Reference Books:

1. Wilfried Voss, “A Comprehensible Guide to Controller Area Network”, Copperhill Media
2. Corporation, 2nd Edition, 2005.
3. Serial Front Panel Draft Standard VITA 17.1 – 200x

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – II Sem.

SYSTEM ON CHIP DESIGN
(Elective-V)

Subject Code: 22MVL1017

L	T	P	C
3	0	0	3

Course Objectives:
The student will be able to
- Understand the components of system, hardware and software.
- Know the basic concepts of processor architecture and instructions.
- Describe external and internal memory of SOC.
- Get knowledge of bus models of SOC
- Understand SOC customization and reconfiguration technologies
- Explain SOC design approach.

Course Outcomes::
At the end of the course the student will be able to
CO 1. Memorize the system architecture, components of system hardware and software.
CO 2. Know the basic concepts of processor architecture and instructions and delays.
CO 3. Describe external and internal memory of SOC and organization.
CO 4. Explain bus architectures and models of SOC.
CO 5. Know SOC customization and reconfiguration technologies.
CO 6. Apply the knowledge of SOC design in real time applications

UNIT –I:
Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity

UNIT –II:
Processors: Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT –III:
Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation, SOC Memory System, Models of Simple Processor – memory interaction.

UNIT -IV:
Interconnect : Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time.

UNIT –V:

SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT –VI:

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

Text Books:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2 nd Ed., 2000, Addison Wesley Professional.

Reference Books:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – II Sem.

HARDWARE & SOFTWARE CO-DESIGN
(Elective-V)

Subject Code: 22MVL1018

L	T	P	C
3	0	0	3

Course Objectives:

- Learn basic concepts of Hardware software Co-design
- Know the Co-design Models, Algorithms and methodology etc…
- Understand Embedded Architectures, Embedded Software Development needs
- Understand Compilation Technologies.
- Learn the Design specification and verification.
- Know the System-level performance modeling, low-level performance modeling and High-level synthesis

Course Outcomes:

CO 1. Analyze any embedded system's hardware and software design issues
CO 2. Choose different Co-design Models, Algorithms and methodology etc., for embedded design
CO 3. Apply Embedded Software Development tools, Compilation Techniques for embedded applications
CO 4. Test the hardware and software individually
CO 5. Explain the System-level performance modeling.
CO 6. Analyze low-level performance modeling and High-level synthesis

UNIT - I:

CO- DESIGN ISSUES AND CO- SYNTHESIS ALGORITHMS: Co - Design Models,Architectures, Languages, a Generic Co-Design Methodology, Hardware – Software Synthesis Algorithms: Hardware – Software Partitioning, Distributed System Co-Synthesis.

UNIT - II:

PROTOTYPING AND EMULATION: Prototyping and Emulation techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping.

UNIT - III:

TARGET ARCHITECTURES: Architecture Specialization Techniques, System Communication infrastructure, Target Architectures and Application System Classes, Architectures for Control Dominated System and Data – Dominated Systems.

UNIT - IV:

COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES: Modern Embedded Architectures, Embedded Software Development needs, Compilation, Technologies, Practical Consideration in a compiler Development Environment.

UNIT - V:

DESIGN SPECIFICATION AND VERIFICATION: Design, Co- Design, The Co- Design Computational Model, Concurrency, coordinating Concurrent Computations, interfacing components, Design Verification, Implementation Verification, Verification Tools, Interface Verification

UNIT - VI:

LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN: System – Level Specification, Design representation for system level synthesis, System level Specification Languages, Heterogeneous Specifications and Multi Language Co – Simulation. The cosyma system and Lycos system.

Text Books:

1. Hardware / Software Co – Design Principles and Practice- Jorgen Staunstrup, Wayne Wolf- 2009, Springer

Reference Books:

1. Hardware / Software Co – Design Principles and Practice, Kluwer Academic Publishers

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M.Tech (VLSI System Design) – II Sem

SYSTEM MODELING & SIMULATION
(Elective-V)

Subject Code: 22MVL1019

L	T	P	C
3	0	0	3

Course Objectives:

- Define the basics of simulation modeling and replicating the practical situations in organizations
- Understand simulation software and packages
- Develop simulation model using heuristic methods.
- Analysis of different simulation processes and Markov Process
- Explain Even Driven Models
- Analysis various System Optimization

Course Outcomes:

CO 1. Analyze the basics of simulation modeling and replicating the practical situations in organizations
CO 2. Choose simulation software and packages
CO 3. Apply simulation model using heuristic methods.
CO 4. Test different simulation processes and Markov Process
CO 5. Analyze Even Driven Models
CO 6. Analyze System Optimization

UNIT – I:

Basic Simulation Modeling: Systems, Models and Simulation, Discrete Event Simulation, Simulation of Single server queuing system, Simulation of Inventory System, Alternative approach to modeling and simulation.

UNIT – II:

SIMULATION SOFTWARE: Comparison of simulation packages with Programming Languages, Classification of Software, Desirable Software features, General purpose simulation packages – Arena, Extend and others, Object Oriented Simulation, Examples of application oriented simulation packages.

UNIT – III:

BUILDING SIMULATION MODELS: Guidelines for determining levels of model detail, Techniques for increasing model validity and credibility.

MODELING TIME DRIVEN SYSTEMS: Modeling input signals, delays, System Integration, Linear Systems, Motion Control models, numerical experimentation.

UNIT – IV:

EXOGENOUS SIGNALS AND EVENTS: Disturbance signals, state machines, petri nets & analysis, System encapsulation.

MARKOV PROCESS: Probabilistic systems, Discrete Time Markov processes, Random walks, Poisson processes, the exponential distribution, simulating a poison process, Continuous – Time Markov processes.

UNIT – V:

EVEN DRIVEN MODELS: Simulation diagrams, Queuing theory, simulating queuing systems, Types of Queues, Multiple Servers.

UNIT – VI:

SYSTEM OPTIMIZATION: System identification, Searches, Alpha/beta trackers, multidimensional optimization, modeling and simulation methodology.

Text Books:

1. System Modeling & Simulation, An introduction – Frank L.Severance, John Wiley&Sons, 2001.
2. Simulation Modeling and Analysis – Averill M.Law, W.David Kelton, TMH, 3rd Edition, 2003.

Reference Books:

1. Systems Simulation – Geoffery Gordon, PHI, 1978.

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – II Sem.

INDUSTRIAL SAFETY
(Open Elective)

Subject Code: 22MOE1001

L	T	P	C
3	0	0	3

Course Outcomes:

At the end of the course, the student should be able to

CO 1. Understand the types, causes and preventive steps of mechanical and electrical hazards.
CO 2. Identify types of maintenance and apply relevant tools of maintenance.
CO 3. Understand the types, causes, applications of wear and types and prevention methods of corrosion
CO 4. Understand the concepts of fault tracing and decision tree for different machine tools
CO 5. List the applications of periodic maintenance.
CO 6. Illustrate the applications of preventive maintenance.

UNIT-I:

Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and fire fighting, equipment and methods.

UNIT-II:

Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

UNIT-III:

Wearand Corrosionandtheirprevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

UNIT-IV:

Fault tracing: Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment's like, i. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

UNIT-V:

Periodicand preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric

motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance.

UNIT-VI:

Procedureforperiodicand preventive maintenance

Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

Text Books:

1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services.
2. Maintenance Engineering, H. P. Garg, S. Chand and Company.

Reference Books:

1. Pump-hydraulic Compressors, Audels, Mcgrew Hill Publication.
2. Foundation Engineering Handbook, Winterkorn, Hans, Chapman & Hall London.

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – II Sem.

OPERATIONS RESEARCH
(Open Elective)

Subject Code: 22MOE1002

L	T	P	C
3	0	0	3

Course Outcomes:
On completion of this course, students should be able to
CO 1. Formulate, solve linear programming problem using graphical and simplex method along with its Big-M and 2-Phase variations.
CO 2. Solve both balanced and unbalanced transportation and assignment problems.
CO 3. Students should able to apply the concept of non-linear programming
CO 4. Compute queue performance characteristics for various queuing models.
CO 5. Solve game theory problems by applying standard solution methods.
CO 6. Calculate critical path for a given network using PERT and CPM techniques.

UNIT-I:
Linear Programming: Introduction to linear programming problem formulation, Graphical solution, Simplex method, Artificial variables techniques, Degeneracy.

UNIT-II:
Transportation Problem: Formulation, Optimal solution, unbalanced transportation problems, Degeneracy.
Assignment Problem: Formulation, Optimal solution, Traveling salesman problem.

UNIT-III:
Nonlinear Programming Problems: Nonlinear programming problem - Kuhn-Tucker conditions min cost flow problem.

UNIT-IV:
Queuing Theory: Characteristics of Queuing models, Classification, (M/M/1):(FCFS/∞/∞), (M/M/1):(FCFS/N/∞), (M/M/C):(FCFS/∞/∞) models.

UNIT-V:
Theory of Games: Introduction, Two-person Zero-sum games, Maximum-Minimax principle, Games without saddle points, Mixed Strategies, m x 2 & 2 x n games, Graphical solutions, Dominance property, Algebraic solutions to rectangular games.

UNIT-VI:
Network models: Project network, CPM and PERT, Critical path scheduling, Cost considerations in project scheduling.

Text Books:

1. Introduction to Operations Research by Prem Kumar Gupta, D.S. Hira, S. Chand Publishers
2. Operations Research, S.D.Sharma, Kedarnath Ramanadh Pub.

Reference Books:

1. Operations Research, J.K. Sharma, MacMilan Pub.
2. Operations Research by P. Rama Murthy, New Age Pub.
3. CPM & PERT, L.S. Srinath, Affiliated East West Press Pu

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – II Sem.

COMPOSITE MATERIALS
(Open Elective)

Subject Code: 22MOE1003

L	T	P	C
3	0	0	3

Course Outcomes:
On completion of this course, students should be able to
CO 1. Illustrate the concept and classification of composites
CO 2. Understand fundamental fabrication processes for polymer matrix,
CO 3. Analyze the strengthening mechanism and structural effect on properties of composite materials.
CO 4. Understand the fundamental concepts of metal matrix, and ceramic matrix composites
CO 5. Understand and Predict elastic properties of long fiber and short fiber composites.
CO 6. Design different types of composite by apply the micromechanics principles.

UNIT - I:
Introduction: Definition – Classification and characteristics of Composite materials. Advantages and application of composites. Functional requirements of reinforcement and matrix. Effect of reinforcement (size, shape, distribution, volume fraction) on overall composite performance.

UNIT – II:
Reinforcements and the reinforcement matrix interface: natural fibers; synthetic organic fibers– aramid, polyethylene; and synthetic inorganic fibers – glass, alumina, boron, carbon, silicon based fibers; particulate and whisker reinforcements, reinforcement-matrix interface – wettability, interfacial bonding, and methods for measuring bond strength.

UNIT - III
Metal Matrix Composites: Introduction, important metallic matrices; metal matrix composite processing: solid state processing – diffusion bonding, powder metallurgy; liquid state processing – melt stirring, compocasting (rheocasting), squeeze casting, liquid infiltration under gas pressure; deposition – spray co-deposition and other deposition techniques like CVD and PVD; in situ processes. Interface reactions.
Properties of MMCs – physical properties; mechanical properties like elastic properties, room temperature strength and ductility, properties at elevated temperatures, fatigue resistance.

UNIT – IV:
Ceramic Matrix Composites: Introduction; processing and structure of monolithic materials – technical ceramics, glass-ceramics. Processing of ceramics: conventional mixing and pressing – cold pressing and sintering, hot pressing, reaction bonding processes, techniques involving slurries, liquid state processing – matrix transfer moulding, liquid infiltration, sol-gel processing, vapour deposition techniques like CVD, CVI, liquid phase sintering, lanxide process and in situ processes. Processing, properties and applications of alumina matrix composites - SiC whisker reinforced, zirconia toughened alumina; Glass-ceramic matrix composites; Carbon-carbon composites - porous carbon-carbon composites, dense carbon-carbon composites.

UNIT – V:

Polymer Matrix Composites: Introduction; polymer matrices – thermosetting, thermoplastic, rubbers. Processing of PMCs , Processing, properties and applications of fibre-reinforced epoxies, PEEK matrix composites, rubber matrix composites. Damping characteristics. Environmental effects in polymer matrix composites. Recycling of PMCs.

UNIT-VI:

Micromechanics of unidirectional composites: micromechanics models for stiffness – longitudinal stiffness, transverse stiffness, shear modulus, Poisson's ratio.

Text Books:

1. Composite Materials: Engineering and Science, by Matthews and Rawlings, CRC Press.
2. Materials Science and Engineering, An introduction. WD Callister, Jr., Adapted by R. Balasubramaniam, John Wiley & Sons, NY, Indian edition, 2007.

Reference Books:

1. Composite Materials Science and Engineering, K.K.Chawla, Springer.
2. An Introduction to composite material, by D.Hull and T.W. Clyne, Cambridge University press.
3. Metal Matrix Composites, Thermomechanical Behaviour by M.Taya, and R.J.Arsenault, Pergamon Press, Oxford.
4. Fundamentals of Metal Matrix Composites by S.Suresh, A.Martensen, and A.Needleman, Butterworth, Heinemann
5. Engineering Materials and Their Applications – R. A Flinn and P K Trojan / Jaico Books.

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – II Sem.

WASTE TO ENERGY
(Open Elective)

Subject Code: 22MOE1004

L	T	P	C
3	0	0	3

Course Outcomes:
At the end of the course, students will be able to:
CO 1. Diagnosis the different wastes and their conversion devices.
CO 2. Assess the diverse pyrolysis types of biomass and production methods of different fuel oils.
CO 3. Evaluate the gasification methods of biomass, their design, construction and operation.
CO 4. Suggest the combustion processes of biomass, their design, construction and operation.
CO 5. Analyze the types of biogas plants.
CO 6. Design and develop the biomass conversion processes.

UNIT-I:
Introduction to Energy from Waste: Classification and Characterization of waste as fuel – Agro based, Forestresidue, Industrial waste – Municipal Solid Waste Conversion devices – Incinerators, gasifiers, digesters.

UNIT-II:
Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods -Yields and application – Manufacture of pyrolytic oils and gases, yields and applications- Oil from waste plastics - Alcohol production from biomass - Bio diesel production.

UNIT-III:
Biomass Gasification: Gasifiers – Fixed bed system – Downdraft and updraft gasifiers –Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation.

UNIT-IV:
Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs,fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

UNIT-V:
Biogas: Properties of biogas (Calorific value and composition) - Types of biogas Plants – Applications - Technologyand status of Biogas plants - Bio energy system - Design and constructional features - Biomass energy program in India.

UNIT-VI:
Biomass: Biomass resources and their classification - Biomass conversion processes – Thermo-chemical conversion - Direct combustion - biomass gasification - pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Urban waste to energy conversion.

Text Books:

1. Rogoff, M.J. and Screve, F., "Waste-to-Energy: Technologies and Project Implementation", Elsevier Store - Reprint - 2011.
2. Hall, D.O. and Overeed, R.P.," Biomass - Renewable Energy", John Willy and Sons – Reprint- 1987.
3. Harker, J.H. and Backhusrt, J.R., "Fuel and Energy", Academic Press Inc – Reprint - 1981.
4. EL-Halwagi, M.M., "Biogas Technology- Transfer and Diffusion", Elsevier Applied Science– Reprint - 1984.

Reference Books:

1. Non-Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 1990.
2. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., Vol. I & II, Tata McGraw Hill Publishing Co. Ltd., 1983.
3. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley & Sons, 1996.
4. Mondal, P. and Dalai, A., "Utilization of natural resources", CRC Press – Published – 2017.
5. Young G.C., "Municipal Solid Waste to Energy Conversion processes", John Wiley and Sons– Reprint – 2010.

Aditya Institute of Technology and Management, Tekkali
(Autonomous)
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – II Sem.

MIXED SIGNAL IC DESIGN LABORATORY

Subject Code: 22MVL1103

L	T	P	C
0	0	4	2

Course Outcomes:

CO 1. Design layouts for various combinational logic circuits and logic functions.
CO 2. Examine mixed signal design flow
CO 3. Design Analog Circuits Simulation using Spice Software
CO 4. Analyze Layout Extraction for Analog & Mixed Signal Circuit.
CO 5. Analyze Parasitic Values from Layout.
CO 6. Measure frequency response, harmonic and inter modulation distortion, and noise behavior

By considering suitable complexity Mixed-Signal application based circuits (circuits consisting of both analog and digital parts), the students are required to perform the following aspects using necessary software tools:

1. Analog Circuits Simulation using Spice Software.
2. Digital Circuits Simulation using Xilinx Software.
3. Mixed Signal Simulation Using Mixed Signal Simulators.
4. Layout Extraction for Analog & Mixed Signal Circuits.
5. Parasitic Values Estimation from Layout.
6. Layout Vs Schematic.
7. Net List Extraction.
8. Design Rule Checks.