AR- 26

COURSE STRUCTURE AND SYLLABI

FOR

M.TECH

VLSI SYSTEM DESIGN

From the Academic Year 2026-2027

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT
(An Autonomous Institution)

Approved by AICTE, New Delhi, Permanently Affiliated to JNTUGV, Vizianagaram, Accredited by NBA and NAAC,

Recognized under 2(f) & 12(B) of UGC

K. Kotturu, Tekkali, Srikakulam – 532 201, Andhra Pradesh.

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT
(AUTONOMOUS)

VISION OF THE INSTITUTE

To evolve into a premier engineering institute in the country by continuously enhancing the range of our competencies, expanding the gamut of our activities and extending the frontiers of our operations.

MISSION OF THE INSTITUTE

Synergizing knowledge, technology and human resource, we impart the best quality education in Technology and Management. In the process, we make education more objective so that efficiency for employability increases on a continued basis.

VISION OF THE DEPARTMENT

Create high-quality engineering professionals through research, innovation and teamwork for a lasting technology development in the area of Electronics and Communication Engineering.

MISSION OF THE DEPARTMENT

M1. To offer a well-balanced Program of instruction, lab practices, research & development activities, product incubation. .

M2: Develop accomplished technical personnel with a strong background on fundamental and advanced concepts, have excellent professional conduct.

M3: Enhance overall personality development which includes innovative and group work exercises, entrepreneur skills, communication skills and employability.

M4: Ensuring effective teaching–learning process to provide in-depth knowledge of principles and its applications pertaining to Electronics & Communication Engineering and interdisciplinary areas.

M5: Providing industry and department interactions through consultancy and sponsored research.

PROGRAM EDUCATIONAL OBJECTIVES

1. **PEO 1**: The graduates will be employed as a practicing engineer in fields such as design, testing and manufacturing.
2. **PEO 2:** The graduates will be able to imbibe research, development and entrepreneurship skills.
3. **PEO 3:** The graduates will be engaged in lifelong self-directed learning to maintain and enhance professional skills.
4. **PEO 4:** The graduates will be able to exhibit communication skills, team spirit, leadership skills and ethics with social responsibility.

PROGRAM OUTCOMES

Engineering Graduates will be able to:

5. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
6. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
7. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
8. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
9. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
10. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant tothe professional engineering practice.

11. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
12. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
13. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
14. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and writeeffective reports and design documentation, make effective presentations, and give and receive clear instructions.
15. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
16. **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES

PSO1. The competency in the application of circuit analysis and design.

PSO2. The ability to solve Electronics and Communication Engineering problems using latest hardware and software tools, along with analytical skills to arrive cost effective and appropriate solutions.

PSO3. The ability to pursue higher studies in either India or abroad and also lead a successful career with professional ethics.

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT
An Autonomous, Tekkali
M.Tech. – VLSI System Design
(AR26 Regulations)
COURSE STRUCTURE

M. Tech. (VLSI System Design) – 1 st SEMESTER						
S.No.	**Subject Code**	**Theory/Lab**	**L**	**T**	**P**	**C**
1	26MVL1001	CMOS Analog Integrated Circuit Design	4	0	0	4
2	26MVL1002	CMOS Digital Integrated Circuit Design	4	0	0	4
3	26MVL1003	Digital Design through Verilog HDL	4	0	0	4
4	**Program Elective–1**					
	26MVL1E11	Semiconductor Memories	3	0	0	3
	26MVL1E12	Embedded system design	3	0	0	3
	26MVL1E13	Quantum Computing	3	0	0	3
5	**Program Elective–2**					
	26MVL1E21	Nano Electronic Materials and Devices	3	0	0	3
	26MVL1E22	Hardware and Software co design of Embedded systems	3	0	0	3
	26MVL1E23	Deep Learning Architectures	3	0	0	3
6	26MVL1101	Analog and Digital Integrated Circuits Design Lab	0	0	4	2
7	26MVL1102	Verilog HDL Programming Lab	0	0	4	2
8	**Audit Course**					
	26MAC1001	English for Research Paper Writing	2	0	0	0
	26MAC1002	Disaster Management				
	26MAC1003	Constitution of India				
Total			**20**	**0**	**8**	**22**

M. Tech. (VLSI System Design) – 2 nd SEMESTER						
S.No.	**Subject Code**	**Theory / Lab**	**L**	**T**	**P**	**C**
1	26MVL1004	Physical Design verification	4	0	0	4
2	26MVL1005	VLSI Testing and Testability	4	0	0	4
3	26MVL1006	CPLD and FPGA Architectures and Applications	4	0	0	4
4	**Program Elective–3**					
	26MVL1E31	Power Management IC Design	3	0	0	3
	26MVL1E32	Advanced Computer Architectures	3	0	0	3
	26MVL1E33	ASIC Design	3	0	0	3
5	**Program Elective–4**					
	26MVL1E41	VLSI Architectures	3	0	0	3
	26MVL1E42	IOT Architecture and Computing	3	0	0	3
	26MVL1E43	Reliability of Devices and Circuits	3	0	0	3
6	26MVL1103	Physical Design Verification Lab	0	0	4	2
7	26MCC1001	Research Methodology and IPR / Swayam 12 week MOOC course – RM&IPR	2	0	0	2
Total			**20**	**0**	**4**	**22**

M. Tech. (VLSI System Design) – 3 rd SEMESTER						
S.No.	**Subject Code**	**Theory/Lab**	**L**	**T**	**P**	**C**
1	26MVL2I01	Internship/ Industrial Training (8 weeks)	-	-	-	3
2	26MVL2201	Technical Seminar	-	-	4	2
3	26MVL2202	Comprehensive Viva	-	-	-	2
4	26MVL2203	DissertationPhase–1	0	0	20	10
Total			**0**	**0**	**24**	**17**

M. Tech. (VLSI System Design) – 4 th SEMESTER						
S.No.	**Subject Code**	**Theory/Lab**	**L**	**T**	**P**	**C**
1	26MVL2204	Dissertation Phase–2	0	0	32	16
Total			**0**	**0**	**32**	**16**

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT
An Autonomous, Tekkali
M. Tech (VLSI System Design) – I Sem.

CMOS ANALOG INTEGRATED CIRCUIT DESIGN

Subject Code: 26MVL1001	L	T	P	C
	4	0	0	4

COURSE OBJECTIVES

- To understand the operation and modeling of MOS transistors in CMOS circuits.
- To design and analyze analog CMOS sub-circuits, such as current mirrors and voltage reference.
- To explore single - stage and multi-stage amplifier designs cascode techniques.
- To study noise behavior in CMOS amplifiers and mitigate its effects.
- To explore CMOS Op amplifiers, two stage Op amplifiers and cascade Op amps

COURSE OUTCOMES

CO 1. Design basic building blocks of CMOS Analog ICs.
CO 2. Carry out the design of single and two stage operational amplifiers and voltage references.
CO 3. Determine the device dimensions of each MOSFET involved.
CO 4. Design various amplifiers like differential, current and operational amplifiers.
CO 5. Design CMOS Op amplifiers, two stage Op amplifiers and cascade Op amps.

UNIT-I

MOS Devices and Modeling: The MOS Transistor, Passive Components - Capacitor &Resistor, Integrated Circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor.

UNIT- II

Analog CMOS Sub-Circuits: MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current Mirror with Beta Helper, Degeneration, Cascode Current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT- III

Single Stage Amplifier: Common Source Stage with Resistive Load, Diode Connected Load, Triode Load, CS Stage with Source Degeneration, Source Follower, CG Stage, Gain Boosting Techniques, Cascode, Folded Cascode.

UNIT- IV

CMOS Amplifiers and Noise: Inverters, Differential Amplifiers, Cascode Amplifiers. Noise - Statistical Characteristics, Types, Noise in Single-Stage Amplifiers, Noise in Differential Pairs, Noise Band width.

UNIT-V

CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of Op Amps.

TEXT BOOKS

1. CMOS Analog Circuit Design-Philip E.Allen and Douglas R.Holberg, Oxford University Press, International Second Edition / Indian Edition, 2010.
2. Design of Analog CMOS Integrated Circuits–Behzad Razavi, TMH Edition.

REFERENCE BOOKS

1. Analog Integrated Circuit Design-David A.Johns, Ken Martin, Wiley Student Edn, 2013.
2. Analysis and Design of Analog Integrated Circuits – Paul R. Gray, Paul J. Hurst, S.Lewis and R.G.Meyer, Wiley India, Fifth Edition,2010.

WEB REFERENCES

1. NPTEL Courses (https://nptel.ac.in/courses/117101105)

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M. Tech (VLSI System Design) – I Sem.

CMOS DIGITAL INTEGRATED CIRCUIT DESIGN

Subject Code: 26MVL1002	L	T	P	C
	4	0	0	4

COURSE OBJECTIVES

- To understand MOSFET operation under static and dynamic conditions for digital design.
- To analyze CMOS inverter characteristics including power, delay, and energy efficiency.
- To design combinational and sequential logic using various CMOS logic styles.
- To explore arithmetic building blocks focusing on speed and are atrade-offs.
- To Analyze memory architectures, focusing on speed and area tradeoffs

COURSE OUTCOMES

CO 1. Analyze and design MOSFET based circuits, focusing on static, dynamic, and power characteristics.
CO 2. Design combinational logic circuits using static CMOS and dynamic logic with optimization techniques.
CO 3. Implement and analyze sequential circuits, including latches, registers, pipelines and timing considerations.
CO 4. Design efficient arithmetic building blocks focusing on speed and area tradeoffs.
CO 5. Analyze memory architectures, focusing on speed and area tradeoffs

UNIT-I

MOS Transistor Principles and CMOS Inverter: MOSFET characteristics under Static and Dynamic Conditions, MOS Transistor Secondary Effects, CMOS Inverter –Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay Parameters, Stick Diagram and Layout Diagrams.

UNIT- II

Combinational Logic Circuits: Static CMOS Design, Different Styles of Logic Circuits, Logical Effort of Complex Gates, Static and Dynamic Properties of Complex Gates, Interconnect Delay, Dynamic Logic Gates.

UNIT- III

Sequential Logic Circuits: Static Latches and Registers, Dynamic Latches and Registers, Timing Issues, Pipelines, Non-Bistable Sequential Circuits.

UNIT- IV

Arithmetic Building Blocks: Data Path Circuits, Architectures for Adders, Accumulators, Multipliers, Speed and Area Tradeoffs.

UNIT-V

Memory Architectures: Memory Architectures and Memory Control Circuits: Read-Only Memories, ROM Cells, Read-Write Memories (RAM), Dynamic Memory Design, 6-Transistor SRAM Cell.

TEXT BOOKS

1. JanRabaey,AnanthaChandrakasan,BNikolic,"DigitalIntegratedCircuits:ADesign Perspective", Prentice Hall of India, 2nd Edition, Feb 2003
2. N.Weste, K.Eshraghian, "Principles of CMOS VLSI Design", AddisionWesley, 2nd Edition, 1993.

REFERENCE BOOKS

1. MJSmith, "Application Specific Integrated Circuits", Addisson Wesley, 1997
2. Sung-MoKang & Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", McGraw-Hill, 1998.

WEB LINKS

1. NPTEL Courses (https://onlinecourses.nptel.ac.in/noc21_ee09/

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An Autonomous, Tekkali
M. Tech (VLSI System Design) – I Sem.

DIGITAL DESIGN THROUGH VERILOG HDL

Subject Code: 26MVL1003	L	T	P	C
	4	0	0	4

COURSE OBJECTIVES

- Learn the design and implementation of the fundamental digital logic circuits using Verilog hardware description language.
- Write the Verilog HDL programming for combinational circuits using different styles of modeling.
- Write the Verilog HDL programming for sequential circuits using different styles of modeling. Design large systems using tasks and functions.
- Design large systems using packages and libraries.

COURSE OUTCOMES

At the end of this course, students will be able to

CO 1. Design and implement the fundamental digital logic circuits using Verilog HDL at various levels of abstractions.
CO 2. Develop the testbench simulation programs for all logic circuits.
CO 3. Design large digital systems based on small modules.
CO 4. Analyze the timing parameters of simulation and synthesis process.
CO 5. Analyze large systems using packages and libraries.

UNIT – I
INTRODUCTION TO VERILOG HDL

Features of verilog HDL, and levels of design description, simulation, test bench simulation, synthesis process.

FUNDAMENTALS OF LANGUAGE ELEMENTS OF VERILOG HDL: Introduction, keywords, identifiers, data types, logic values, scalars and vectors, parameters, memory, operators, and basic system tasks.

UNIT – II
GATE LEVEL MODELING

Introduction, AND gate primitive, Module structure, other gate primitives, tri-state gates, and arrays of instances. Design of basic combinational circuits and flip-flops using gate primitive with delays, signal strengths, contention resolution, and net types.

UNIT – III
DATA FLOW MODELING

Data flow modeling using continuous assignments. assignment statements, delays, vector assignments, and Verilog operators. Design of combinational and simple sequential circuits using data flow modeling.

UNIT – IV
BEHAVIORAL MODELING

Introduction, behavioral and RTL modeling concepts. Procedural blocks (initial, always), blocking and non-blocking assignments, conditional statements (if, if–else, case), looping constructs (for, while, repeat, forever), multiple always blocks, events, and an overview of simulation flow.

UNIT – V

ADVANCED VERILOG AND FSM DESIGN

Advanced Verilog concepts, system tasks and functions, user-defined tasks and functions, parameters and module parameterization, compiler directives, and hierarchical access. The design and implementation of finite state machines using Moore and Mealy models.

TEXT BOOKS

1. DesignthroughVerilogHDL–T.R.PadmanabhanandB.BalaTripuraSundari,WSE,2004 IEEE press.
2. AVerilogPrimer– J.Bhaskar,BSP,2003.

REFERENCE BOOKS

1. Fundamentals of Logic Design with Verilog – Stephen. Brown and ZvonkoVranesic, TMH, 2005.
2. Advanced Digital Design with Verilog HDL–Michael D. Ciletti, PHI, 2005.

WEB LINKS

1. https://onlinecourses.nptel.ac.in/noc24_cs61/preview

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(An Autonomous) TEKKALI
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – I Sem.

SEMI CONDUCTOR MEMORIES

Subject Code: 26MVL1E11	L	T	P	C
	3	0	0	3

COURSE OBJECTIVES

- To explain the concepts and working principles of volatile memories (SRAM, DRAM, multi-ported RAMs, CAMs).
- To describe non-volatile memories (ROM, RRAM, MRAM, Flash, 3D memories).
- To analyze reliability and design issues in semiconductor memories.
- To explore advanced memory technologies, packaging techniques, and emerging trends in memory chip design.
- Explain advanced and emerging memory technologies and high-density packaging solutions.

COURSE OUTCOMES

CO 1. Explain the concepts and working principles of SRAM advanced SRAM Technologies.
CO 2. Explain the concepts and working principles of DRAM advanced DRAM Technologies
CO 3. Describe non-volatile memories (ROM, RRAM, MRAM, Flash, 3D memories).
CO 4. Analyze reliability and design issues in semiconductor memories.
CO 5. Assess advanced and emerging memory technologies and high-density packaging solutions.

UNIT - I

STATIC RANDOM-ACCESS MEMORY TECHNOLOGIES: SRAM Cell Structures, MOS SRAM Architecture and Peripheral Circuit Operation, Bipolar SRAM Technologies, Advanced SRAM Architectures and Technologies, Application Specific SRAMs.

UNIT - II

DYNAMIC RANDOM-ACCESS MEMORIES (DRAMS): DRAM Technology Development, CMOS DRAMs, DRAMs Cell Theory and Advanced Cell Structures, Bi- CMOS DRAMs, Soft Error Failures in DRAMs, Advanced DRAM Designs and Architecture, Application Specific DRAMs.

UNIT - III

NON-VOLATILE MEMORIES: Masked Read-Only Memories (ROMs), High Density ROMs, Programmable Read-Only Memories (PROMs), CMOS PROMs, Erasable (UV) Programmable Read-Only Memories (EPROMs), Floating Gate EPROM Cell, Onetime Programmable (OTP) EPROMs, Electrically Erasable PROMs (EEPROMs), EEPROM Technology and Architecture, Non-Volatile SRAM, Flash Memories (EPROMs or EEPROM).

UNIT - IV

SEMICONDUCTOR MEMORY RELIABILITY AND RADIATION EFFECTS: General Reliability Issues, RAM Failure Modes and Mechanism, Non-volatile Memory Reliability, Modelling and Failure Rate Prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and Qualification, Radiation Effects, Single Event Phenomenon (SEP), Radiation Hardening Techniques and Design Issues.

UNIT - V

ADVANCED MEMORY TECHNOLOGIES AND HIGH-DENSITY PACKAGING: Ferroelectric RAM (FRAM), Gallium Arsenide (GaAs) FRAM, Magneto Resistive RAM (MRAM), Analog Memories, Experimental and Emerging Memory Devices, Memory Hybrids (2D & 3D Architectures), Memory Stacks and 3D Integration, High-Density Memory Packaging Techniques.

TEXT BOOKS

1. Emerging Nanotechnologies (Mark Tehranipoor, 2007).
2. Practice Problems for Hardware Engineers (Nazarian, 2021).

REFERENCE BOOKS

1. AndreiPavlov, Manoj Sach dev, "CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies", Springer Germany, 2008.
2. Ashok K. Sharma, "Semiconductor Memories Technology, Testing and Reliability", Prentice-Hall of India Private Limited, New Delhi, 1997. Fernanda Lima Kastensmidt, Ricardo Reis "Fault-Tolerance Techniques for SRAM-Based FPGAs", Springer US, 2006.

WEB LINKS

1. **NPTEL Courses** www.youtube.com/playlist?list=PLbMVogVj5nJRtXgdjQkYfYOHfsc-7Ar7Q

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ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – I Sem.

EMBEDDED SYSTEM DESIGN

Subject Code: 26MVL1E12	L	T	P	C
	3	0	0	3

COURSE OBJECTIVES

- To provide basic knowledge of embedded systems and their applications.
- To introduce embedded hardware components and firmware concepts.
- To familiarize students with embedded system development tools.
- To introduce real-time operating system concepts and processor architecture support.
- To present embedded system testing methods and design approaches.

COURSE OUTCOMES

CO 1. **Define** the basic concepts, characteristics, and applications of embedded systems.
CO 2. Explain the embedded hardware components, firmware, and communication interfaces.
CO 3. Apply embedded system development tools to build and debug embedded programs.
CO 4. Explain RTOS functions, scheduling, and processor architecture support in real-time embedded systems.
CO 5. Analyze embedded system testing tools and processor-based embedded system designs.

UNIT-I

Embedded System Fundamentals and Life Cycle

Embedded System – Definition, Embedded system versus General computing systems, History of Embedded systems, Classification of Embedded systems, Major application areas of embedded systems, Purpose of embedded systems, Characteristics of an embedded system, Quality attributes of embedded systems, Application-specific and Domain-Specific examples of an embedded system

UNIT-II

Embedded Hardware and Firmware: Analog and digital electronic components, I/O types and examples, Serial communication devices, Parallel device ports, Wireless devices, Timer and counting devices, Watchdog timer, Real-time clock, Embedded Firmware design approaches, Embedded Firmware development languages, Concepts of C versus Embedded C, Compiler versus Cross-compiler.

UNIT-III

Embedded System Development Tools and Process: The integrated development environment, Types of files generated on cross-compilation, Deassembler / Decompiler, Simulators, Emulators and Debugging, Target hardware debugging, Boundary Scan, Embedded Software development process and tools.

UNIT-IV

Real Time Operating Systems: Operating system basics, Types of operating systems, Kernal, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Threads, Processes and Scheduling, Task communication, Task synchronization, Device Drivers, RISC processor architecture support for RTOS and real-time execution.

UNIT-V

Embedded System Testing and Case Studies: The main software utility tool, Translation tools- Pre-processors, Interpreters, Compilers and Linkers, Debugging tools, Testing on host machine, Laboratory Tools.

Case studies- Processor design approach of an embedded system –Power PC Processor based and Micro Blaze Processor based embedded system design.

TEXTBOOKS

1. Introduction to Embedded Systems by Shibu K.V., Tata McGraw Hill Education, 2013
2. Embedded System Design by Frank Vahid and Tony Givargis, John Wiley & Sons, 2002.

REFERENCES

3. Embedded Systems Architecture: A Comprehensive Guide for Engineers and Programmers - Tammy Noergaard, Second Edition, Elsevier (Singapore) Private Limited Publications, 2005.
4. Embedded Systems: Architecture, Programming and Design - Rajkamal, TMH, Second Edition, 2008.

WEB LINKS

1. https://www.tutorialspoint.com/embedded_systems/index.htm
2. https://www.freertos.org/Documentation/RTOS_book.html
3. https://www.tutorialspoint.com/software_testing/software_testing_quick_guide.htm

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(An Autonomous) TEKKALI
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – I Sem.

QUANTUM COMPUTING

Subject Code: 26MVL1E13	L	T	P	C
	3	0	0	3

COURSE OBJECTIVES

After completing this course the student will be able to:

- Understand the fundamental principles of quantum mechanics required for quantum computation (qubits, superposition, entanglement, measurement).
- Model and analyze quantum gates, circuits and basic quantum algorithms using linear algebra and Dirac notation.
- Design and evaluate key quantum algorithms (e.g., Deutsch-Jozsa, Grover, Shor) and assess their computational advantages.
- Study quantum error sources, basic quantum error correction and fault-tolerant concepts relevant to VLSI-style hardware mapping.
- Gain practical familiarity with quantum programming toolkits and cloud quantum backends for small-scale experiments and simulations.

Course Outcomes:

On successful completion, the student will be able to:

CO 1. Explain the mathematical formalism of qubits and quantum operations and apply it to analyze simple quantum systems.

CO 2. Construct and simulate quantum circuits for canonical algorithms and reason about their complexity relative to classical counterparts.

CO 3. Apply quantum error correction codes and describe requirements for fault tolerance in hardware implementations.

CO 4. Use quantum SDKs to implement, simulate and debug small quantum circuits; interpret results from real or simulated quantum devices.

CO 5. Critically evaluate current quantum hardware architectures and propose VLSI-inspired design considerations for hybrid quantum–classical systems.

UNIT-I

Foundations and Linear Algebra for Quantum Computing: Complex vector spaces, inner products, tensor products, Dirac notation. Qubits, Bloch sphere representation, pure and mixed states (density matrices). Quantum postulates: state evolution, measurement, composite systems. Single-qubit gates: Pauli, Hadamard, phase, rotation gates; multi-qubit basics. Review of computational complexity basics (P, NP, BQP intuition).

UNIT-II

Quantum Gates, Circuits and Entanglement: Multi-qubit gates: CNOT, CZ, SWAP, Toffoli, controlled-U. Universal gate sets and decomposition. Entanglement: EPR pairs, Bell states, GHZ states; measures of entanglement. Quantum circuit model, circuit identities, circuit depth and width tradeoffs. Teleportation, superdense coding, and simple protocols.

UNIT-III

Quantum Algorithms: Deutsch and Deutsch–Jozsa algorithms — problem statement and circuit analysis. Shor's factoring algorithm — high-level flow, period finding via QFT. Grover's search algorithm — amplitude amplification and complexity. Other algorithms: Phase estimation, quantum simulation basics.

UNIT-IV

Noise, Error Correction and Fault Tolerance: Sources of errors in quantum hardware; decoherence, relaxation, dephasing, gate errors. Quantum operations formalism (Kraus operators) and noise models. Basic quantum error correction (QEC): bit-flip, phase-flip, Shor code, Steane code. Fault tolerance principles & thresholds (conceptual)

UNIT-V

Quantum Hardware, VLSI Considerations & Programming: Overview of physical qubit technologies: superconducting qubits, trapped ions, spin qubits — strengths & constraints. Qubit connectivity, crosstalk, control electronics and cryogenics. Mapping quantum circuits to hardware: qubit routing, SWAP insertion, layout and timing constraints (VLSI analogy). Quantum programming toolkits: circuit design, simulator vs real backend.

TEXTBOOKS

1. Quantum Computation and Quantum Information — M. A. Nielsen and I. L. Chuang.
2. Quantum Computing: A Gentle Introduction — Eleanor Rieffel and Wolfgang Polak.
3. Quantum Computer Science: An Introduction— N. David Mermin.

REFERENCE TEXTBOOKS

1. An Introduction to Quantum Computing— P. Kaye, R. Laflamme, and M. Mosca.
2. Quantum Computing: An Applied Approach— J. Hidary.

WEB LINKS

1. https://ocw.mit.edu/](https://ocw.mit.edu/
2. https://qiskit.org/textbook
3. https://qiskit.org/textbook
4. https://learn.microsoft.com/quantum
5. https://learn.microsoft.com/quantum

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M. Tech (VLSI System Design) – I Sem.

NANO ELECTRONIC MATERIALS AND DEVICES

Subject Code: 26MVL1E21	L	T	P	C
	3	0	0	3

COURSE OBJECTIVES

- To gain knowledge of synthesis, characterization, and fabrication techniques for semiconductor nano materials.
- To understand fundamental physics of electron transport, optical processes, and semiconductor interfaces at the nano scale.
- To analyze scaling challenges in MOSFETs and explore advanced transistor architectures for nano electronics.
- To explore the design and operation of emerging nano electronic and optoelectronic devices.
- To investigate next-generation semiconductor technologies including solar cells, LEDs, and advanced memory devices.

COURSE OUTCOMES

At the end of the course, the student will be able to

CO 1. Explain synthesis routes and characterization methods for nano materials (XRD, SEM, TEM, UV-VIS, XPS).

CO 2. Compare nanofabrication techniques such as CVD, PECVD, ALD, and MBE for device applications.

CO 3. Differentiate diffusive vs. ballistic transport and evaluate semiconductor interface physics in MOS structures.

CO 4. Apply MOS scaling theory to identify short-channel effects and assess advanced transistor designs (FinFET, Surround Gate FET).

CO 5. Analyze and evaluate the physics of nanoelectronic devices, optoelectronic structures, and next-generation semiconductor technologies (solar cells, LEDs, Fe-RAM, R-RAM).

UNIT – I

Nano Electronic Materials: Synthesis of semiconductor nano materials (0D, 1D, 2D): nano precipitation routes, Sol-gel method. Characterization of nano materials using XRD, SEM, TEM, UV-VIS spectroscopy, XPS.

Nanofabrication: physical and chemical vapor deposition methods (PECVD & CVD), atomic layer deposition (ALD), molecular beam epitaxy (MBE), Flip-chip bonding and advanced packaging.

UNIT – II

Nano Semiconductor physics: Transport in nanostructures, Electron flow in solids, diffusive and ballistic electron transport, injection velocity, velocity overshoot, hall-effect and quantum hall-effect, optical and electro-optic processes in hetero structures.

Physics of semiconductor interface: Metal-Insulator, Metal-Semiconductor, and Metal-Oxide-Semiconductor (MOS) Junction physics.

UNIT – III

MOSFETs at nano scale: MOS scaling theory, Issues in scaling MOSFETs, short channel effects, Requirements for non-classical MOSFET. Metal gate transistor: Motivation, requirements, Integration Issues, gate transistors, integration issues, Vertical transistors - FinFET and Surround gate FET.

UNIT – IV

Nano electronic devices: hot electron transistors, single electron transistors, resonant tunnelling transistors, low dimensional semiconductor lasers: quantum-well lasers, quantum dot lasers, low dimensional photo detectors.

UNIT – V

Next generation semiconductor devices: Physics of organic solar cells (OSCs), organic light emitting diodes (OLED), advanced memory device physics: ferroelectric, and resistive memory devices, Introduction to chip let and their integration in next-generation devices.

TEXT BOOKS

1. Nano Technology and Nano Electronics-Materials, devices and measurement Techniques by WR Fahrner - Springe.
2. Encyclopedia of Materials Characterization, Edited by: Brundle, C.Richard; Evans, Charles A. Jr.; Wilson, Shaun; Elsevier.

REFERENCE BOOKS

1. G. Cao, Nanostructures and Nonmaterial's – Synthesis, Properties and Applications, Imperial College Press 2006
2. Physical Principles of Electron Microscopy, R.F. Egerton (Springer)

WEB LINKS

1. https://www.youtube.com/watch?v=Oq5TweDVyKQ

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT
(An Autonomous) TEKKALI
ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – I Sem.

HARDWARE AND SOFTWARE CO-DESIGN OF EMBEDDED SYSTEMS

Subject Code: 26MVL1E22	L	T	P	C
	3	0	0	3

COURSE OBJECTIVES

- Introducing hardware–software co-design concepts and design methodology.
- To provide knowledge of prototyping, emulation techniques, and target architectures for embedded systems.
- To familiarize students with embedded processor architectures and compilation techniques.
- Introducing system-level design concepts and verification methods in embedded systems.
- Present system-level specification languages and multi-language co-simulation concepts.

COURSE OUTCOMES

CO 1. Explain hardware–software co-design concepts and co-synthesis methods in embedded systems.
CO 2. Describe prototyping, emulation techniques, and target architectures for embedded systems.
CO 3. Explain compilation techniques and development tools for embedded processor architectures.
CO 4. Explain design specification, concurrency, and verification methods in embedded systems.
CO 5. Describe system-level specification languages and multi-language co-simulation in embedded systems.

UNIT - I

Co- Design Issues & Hardware/Software Co- Synthesis Algorithms: Co- Design Issues: co-design models, architectures, languages, a generic co-design methodology. Hardware/software co-synthesis algorithms: introduction, preliminaries, architectural model hardware – software partitioning, distributed system co-synthesis.

UNIT – II

Prototyping and Emulation: Prototyping and emulation techniques, proto typing and emulation environments, future developments in emulation and prototyping, system communication infrastructure.

Target Architectures: Architecture specialization techniques, target architecture and application system classes, architecture for control dominated systems (8051-architectures for high-performance control), architecture for data dominated systems (adsp21060, tms320c60),and mixed systems

UNIT - III

Compilation Techniques and Tools for Embedded Processor Architectures: Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

UNIT – IV

Design Specification and Verification: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, and interface verification

UNIT – V

Languages for System – Level Specification and Design: System – level specification, design representation for system level synthesis, systemlevel specification languages, heterogeneous specifications and multi-language co-simulation.

TEXTBOOKS

1. I Jorgen Staunstrup, Wayne Wolf, Hardware / software co- design Principles and Practice, Springer, 2009.
2. Kluwer, Hardware / software co- design Principles and Practice, academic publishers, 2002.

REFERENCES

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer Publications.
2. Frank Vahid and Tony Givargis, Embedded System Design: A Unified Hardware/Software Introduction, Wiley, 2002.

WEB LINKS

1. https://nptel.ac.in/courses/106103182
2. https://inst.eecs.berkeley.edu/~ee249/sp02/

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ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – I Sem.

DEEP LEARNING ARCHITECTURES

Subject Code: 26MVL1E23	L	T	P	C
	3	0	0	3

COURSE OBJECTIVES

After completing this course, the student will be able to:

- Develop strong mathematical foundations required for deep learning including linear algebra, probability, optimization, and generalization principles.
- Understand and analyse convolutional neural network architectures and their evolution for computer vision applications.
- Design and evaluate deep learning models for detection, segmentation, and efficient deployment in real-world systems.
- Analyze sequence modelling techniques including RNNs, LSTMs, GRUs, and Transformer architectures for language and temporal data processing.
- Explore advanced deep learning paradigms such as Graph Neural Networks, generative models, diffusion models, and robustness techniques.

COURSE OUTCOMES

Upon successful completion of the course, students will be able to:

CO 1. Apply optimization algorithms and regularization techniques to train deep neural networks effectively.
CO 2. Compare and implement modern CNN architectures for image classification and vision tasks.
CO 3. Design deep learning models for object detection, segmentation, and resource-efficient deployment.
CO 4. Implement sequence models and Transformer-based architectures for language and sequential data applications.
CO 5. Analyze advanced architectures such as GNNs and generative models, and evaluate model robustness and reliability.

UNIT-I

Mathematical Foundations & Optimization: Review of Linear Algebra: vectors, matrices, eigenvalues, SVD. Probability & Information Theory: random variables, entropy, KL divergence. Fundamentals of Deep Learning: Perceptron, Multi-Layer Perceptron (MLP). Activation functions: Sigmoid, Tanh, ReLU, variants. Weight initialization techniques. Batch Normalization and Layer Normalization. Loss functions: MSE, Cross-Entropy, Hinge Loss. Regularization: L2, Dropout, Early stopping. Generalization and bias–variance tradeoff. Optimization algorithms: SGD, Momentum, RMSProp, Adam. Convergence intuition and hyper parameter tuning strategies.

UNIT-II

Convolutional Neural Networks & Core Vision Architectures: Convolution operation, feature maps, receptive field. Padding, stride, pooling operations. Dilated convolution and separable convolution. Classic architectures evolution: LeNet → AlexNet → VGG → ResNet (identity & bottleneck blocks) → DenseNet. Modern CNN building blocks: Residual connections, Group convolution, Depthwise separable convolution, Squeeze-and-Excitation blocks.

UNIT-III

Detection, Segmentation & Efficient Vision Models: Object Detection overview: R-CNN, Fast R-CNN, Faster R-CNN. YOLO and SSD concepts. Semantic & instance segmentation overview: U-Net architecture. Efficient architectures for deployment: MobileNet, EfficientNet. Vision Transformers (ViT) and hybrid CNN-Transformer models (conceptual introduction).

UNIT-IV

Sequence Models & Transformer Architectures: Recurrent Neural Networks: Vanilla RNN. LSTM and GRU — gating mechanisms. Training challenges: vanishing/exploding gradients. Sequence modeling tasks: language modeling, sequence-to-sequence learning. Attention mechanisms. Transformers: Self-attention, Multi-head attention, Positional encoding. Encoder–decoder stacks. Pretraining & fine-tuning paradigms (high-level overview of BERT/GPT families). Scaling laws in deep learning.

UNIT-V

Advanced & Emerging Architectures: Graph Neural Networks (GNNs): Message passing framework, GCN, GAT. Generative models: Autoencoders, Variational Autoencoders (VAEs), GAN basics. Diffusion models (conceptual overview). MLP-Mixer architecture. Robustness in deep learning. Adversarial examples and defenses. Model calibration and reliability.

TEXT BOOKS

1. Deep Learning — Ian Goodfellow, Yoshua Bengio, Aaron Courville.
2. Deep Learning with Python — François Chollet.
3. Hands-On Machine Learning with Scikit-Learn, Keras, and TensorFlow — AurélienGéron.

REFERENCE BOOKS

1. Pattern Recognition and Machine Learning — Christopher M. Bishop.
2. Neural Networks and Learning Machines — Simon Haykin.
3. Neural Networks and Deep Learning — Michael Nielsen.

ONLINE RESOURCE LINKS

http://cs231n.stanford.edu/](http://cs231n.stanford.edu/
https://jalammar.github.io/illustrated-transformer/
https://jalammar.github.io/illustrated-transformer/
https://www.tensorflow.org/model_optimization
https://www.tensorflow.org/model_optimization
https://pytorch.org/docs/stable/quantization.html
https://pytorch.org/docs/stable/quantization.html

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ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – I Sem.

ANALOG AND DIGITAL INTEGRATED CIRCUITS DESIGN LAB

Subject Code: 26MVL1101	L	T	P	C
	0	0	4	2

COURSE OBJECTIVES

- To understand **CMOS analog and digital circuit design principles** using industry-standard EDA tools.
- To develop **schematics and layouts** for analog and digital CMOS circuits following full-custom IC design methodologies.
- To analyze the **performance, functionality, and optimization** of CMOS circuits through simulation.
- To apply **physical verification techniques**, including layout extraction, DRC, and LVS, to ensure design correctness.
- To gain hands-on experience in **pre-layout and post-layout simulations** for validating CMOS circuit designs.

COURSE OUTCOMES

After completing the course, students will be able to:

CO 1. Apply **VLSI design methodologies** using industry-standard tools such as Mentor Graphics, Cadence, or Synopsys.
CO 2. Design and analyze **CMOS analog and digital circuits** for full-custom integrated circuit applications.
CO 3. Perform **layout extraction and physical verification** to ensure functionality and manufacturability of CMOS designs.
CO 4. Conduct **pre-layout and post-layout simulations** to validate and optimize circuit performance.
CO 5. Evaluate and optimize **CMOS circuit performance parameters**, including speed, power, and area, for analog and digital systems.

LIST OF EXPERIMENTS

1. MOS Device Characterization and parametric analysis.
2. Common Source Amplifier.
3. Cascode amplifier.
4. Simple current mirror.
5. Cascode current mirror.
6. R-2RLadderTypeDAC.
7. Inverter Characteristics.
8. NAND and NOR Gate.
9. XOR and XNOR Gate.
10. 2:1 Multiplexer.
11. Full Adder.
12. JK-Flip Flop.

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ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – I Sem.

VERILOG HDL PROGRAMMING LAB

Subject Code: 26MVL1102	L	T	P	C
	0	0	4	2

COURSE OBJECTIVES

- Understand the fundamentals of digital logic design and Boolean function realization using Verilog HDL.
- Design and implement combinational circuits such as adders, subtractions, multiplexers, encoders, decoders, comparators, and ALUs.
- Develop sequential circuits including flip-flops, registers, counters, and shift registers using Verilog HDL.
- Model and analyze finite state machines (Mealy and Moore) for digital system design.
- Simulate, synthesize, and verify digital circuits using FPGA design tools and implement them on hardware platforms.

COURSE OUTCOMES

CO 1. Realize Boolean expressions and design combinational logic circuits using Verilog HDL.
CO 2. Design arithmetic and logic circuits such as adders, ALUs, comparators, multiplexers, and decoders with correct functionality.
CO 3. Implement sequential circuits including flip-flops, registers, counters, and universal shift registers.
CO 4. Design and verify Mealy and Moore finite state machines for sequence detection and control applications.
CO 5. Perform simulation, synthesis, and FPGA implementation of digital circuits and analyze \ their functional and timing behavior..

The students are required to simulate, synthesize, and implement the following experimental part on the Verilog environment and Synthesis using Xilinx Vivado using FPGA devices.

LIST OF EXPERIMENTS

1. Realization of a Four-Variable Boolean Function
2. Arithmetic Units (Adders, Subtractors)
3. 8-bit Parallel Adder
4. Multiplexers and Demultiplexers
5. Encoders, Decoders, and Priority Encoder
6. Four-bit Digital Comparator
7. Arithmetic Logic Unit (ALU)
8. Waveform Generators
9. Flip-Flops
10. Registers and Counters
11. Universal Shift Register (Serial In–Serial Out, Serial In–Parallel Out, Parallel In–Serial Out, Parallel In–Parallel Out)
12. Mealy and Moore State Machines

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ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – I Sem.

ENGLISH FOR RESEARCH PAPER WRITING

Subject Code: 26MAC1001	L	T	P	C
	2	0	0	0

COURSE OBJECTIVES

- **To develop students' ability to plan and organize academic writing** by mastering word order, sentence structure, paragraph development, conciseness, and techniques for avoiding ambiguity and redundancy.
- **To enable learners to present ideas clearly and responsibly** through skills such as clarifying agency (who did what), highlighting findings, using hedging and criticism appropriately, and avoiding plagiarism through effective paraphrasing.
- **To train students in the structure and components of a research paper** by understanding and producing well-organized abstracts, introductions, literature reviews, methods, results, discussions, and conclusions.
- **To enhance students' competence in writing key academic sections**—including titles, abstracts, introductions, and literature reviews—using appropriate academic style, coherence, and logical progression.
- **To equip learners with practical skills for drafting, revising, and finalizing research papers** by applying section-specific writing strategies and conducting a thorough final check for clarity, accuracy, and academic integrity.

COURSE OUTCOMES

CO 1. **Students will be able to plan and organize academic texts effectively** by applying correct word order, clear sentence and paragraph structure, and techniques for conciseness while avoiding ambiguity and redundancy.

CO 2. **Students will be able to present information clearly and ethically** by clarifying agency (who did what), highlighting key findings, using appropriate hedging and criticism, and avoiding plagiarism through accurate paraphrasing.

CO 3. **Students will be able to write and evaluate major sections of a research paper** such as literature reviews, methods, results, discussions, conclusions, and perform a final check for coherence and accuracy.

CO 4. **Students will be able to construct effective titles, abstracts, and introductions** and develop logically organized reviews of literature using accepted academic writing conventions.

CO 5. **Students will be able to apply section-specific writing skills** to produce well-structured methods, results, discussion, and conclusion sections that meet academic and research communication standards.

SYLLABUS

UNIT-I

Planning and preparation, Word order, Breaking up long sentences, Structuring paragraphs and sentences. Being concise and removing redundancy, Avoiding ambiguity and vagueness

UNIT-II
Clarifying who did what, Highlighting findings. Hedging and criticizing. Paraphrasing and plagiarism, Sections of a paper, Abstracts, Introduction

UNIT-II
Clarifying who did what, Highlighting findings. Hedging and criticizing. Paraphrasing and plagiarism, Sections of a paper, Abstracts, Introduction

UNIT-III
Review of the Literature. Methods, Results, Discussion, Conclusions, Final check

UNIT-IV
Key skills needed when writing a title. An abstract, An introduction and a review of the Literature

UNIT-V
Skills needed when writing methods, Results, Discussions and Conclusion.

TEXT BOOKS
1. Goldbort R (2006). Writing for Science. Yale University Press.
2. Day R (2006). How to Write and Publish a Scientific Paper. Cambridge University Press.
3. Highman N (1998). Handbook of Writing for the Mathematical Sciences. SIAM. Highman's book.

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ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – I Sem.

DISASTER MANAGEMENT

Subject Code: 26MAC1002	L	T	P	C
	2	0	0	0

COURSE OBJECTIVES

The primary objectives of this course are:

- To provide basic concepts and terminologies related to hazards and disasters.
- To highlight the critical importance and role of disaster management in the contemporary world.
- To enhance awareness of institutional processes, policies, and management strategies used to mitigate disaster impacts.
- To analyze the various dimensions of vulnerability and their contribution to disaster risk.
- To equip knowledge regarding emergency management for manmade and technological threats.

COURSE OUTCOMES

Upon successful completion of this course, students will be able to:

CO 1. Define and classify different types of disasters and distinguish them from hazards.
CO 2. Evaluate the nature of vulnerability and assess the impacts of disasters on different communities.
CO 3. Explain the components of the Disaster Management Cycle, including mitigation, preparedness, response, and recovery.
CO 4. Discuss the institutional frameworks and legislations available for disaster risk management at national and international level.
CO 5. Identify specific threats related to industrial accidents and security, and understand the necessary emergency response mechanisms.

UNIT-I

Introduction and Basic Concepts: Understanding Fundamental Concepts: Definitions of Hazards and Disasters. Classification: Disaster types and causes including Geophysical, Hydrological, Meteorological, Biological, Atmospheric, and Human-made. Distinguishing between natural hazards and manmade disasters

UNIT-II

Dimensions of Disasters and Vulnerability: Global Trends: Analysis of global trends in disasters. Impact analysis: Physical, Social, Economic, Political, Environmental, and Psychosocial impacts of disasters. Understanding Vulnerability: Defining and analyzing Physical Vulnerability, Economic Vulnerability, and Social Vulnerability

UNIT-III

The Disaster Management Cycle and Risk Reduction: Detailed study of the components of DM Cycle: Response and recovery, Risk assessment, Mitigation and prevention, Preparedness planning, Prediction and warning. Disaster Risk Reduction (DRR): Concepts of DRR and Community based disaster risk reduction strategies.

UNIT-IV

Institutional Frameworks and Initiatives: National Context: Disaster Risk Management in India; related policies, plans, programs, and legislation. Global Context: International strategies for disaster reduction and other global initiatives. Agencies: Role of agencies NIDM, NDRF.

UNIT-V

Emergency Management and Emerging Threats: Technological and Industrial Disasters: Explosions, Industrial accidents, Nuclear, Transport, and Mining accidents. Environmental Emergencies: Spills (Oil and Hazardous material). Security Threats: Bomb threats, terrorist attacks, stampedes, and conflict situations.

TEXTBOOKS

1. Sharma, S.C., Disaster Management, Khanna Book Publishing. Latest Edition
2. Singh, R. B. (ed.), Natural Hazards and Disaster Management: Vulnerability and Mitigation, Rawat Publications, New Delhi. Latest Edition
3. Modh, S., Managing Natural Disaster: Hydrological, Marine and Geological Disasters, Macmillan, Delhi. Latest Edition

REFERENCE BOOKS

1. **Carter, N.**, Disaster Management: A Disaster Management Handbook, Asian Development Bank, Manila. Latest Edition
2. **Clements, B. W.**, Disasters and Public Health: Planning and Response, Elsevier Inc. Latest Edition
3. **Dunkan, K., and Brebbia, C. A. (Eds.)**, Disaster Management and Human Health Risk: Reducing Risk, Improving Outcomes, WIT Press, UK. Latest Edition
4. **Ramkumar, Mu**, Geological Hazards: Causes, Consequences and Methods of Containment, New India Publishing Agency, New Delhi. Latest Edition

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT
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ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – I Sem.

CONSTITUTION OF INDIA

Subject Code: 26MAC1003	L	T	P	C
	2	0	0	0

COURSE OBJECTIVES

- To provide students with a comprehensive understanding of the historical background and salient features of the Indian Constitution, including Fundamental Rights, Duties, and Directive Principles of State Policy.
- To familiarize learners with the structure and functioning of local self-government institutions and the importance of grassroots democracy in India.
- To develop awareness of the parliamentary system of government in India, including the roles and powers of the President, Prime Minister, Cabinet, and Judiciary.
- To explain the nature of Indian federalism and the legislative procedures and privileges of Union and State legislatures.
- To enable students to understand the role and functioning of constitutional and statutory bodies such as parliamentary committees, Election Commission, CAG, Finance Commission, NITI Aayog, and political parties**.**

COURSE OUTCOMES

CO 1. Students will be able to explain the origin, structure, and key features of the Indian Constitution, including Fundamental Rights, Fundamental Duties, and Directive Principles.

CO 2. Students will be able to describe the organization and functions of local administration, including Panchayati Raj Institutions and municipal bodies, and appreciate the value of participatory democracy.

CO 3. Students will be able to analyze the working of the parliamentary system and the emergency provisions, and understand the relationship between the executive, legislature, and judiciary.

CO 4. Students will be able to interpret the principles of Indian federalism and explain Union–State relations and the legislative process in Parliament and State Legislatures.

CO 5. Students will be able to evaluate the role of constitutional and non-constitutional bodies and **recognize their contribution to democratic governance and accountability in India.**

SYLLABUS

UNIT-I

Introduction: Historical perspective of the constitution of India -Salient features of The Indian Constitution-Features: Fundamental Rights (Article 12 to 35), Duties (31 A-1976 emergency) and Directive principles (Article 30 to 51) of State Policy - Articles 14 to 18 Articles 19-Article 21-Amendment Procedure of The Indian Constitution: 42nd amendment (Mini Constitution)-44th amendment (1978-Janatha Govt.)

UNIT-II

Local Administration: District's administration head: Role and Importance, Municipalities Introduction, Mayer and role of elected representative, CEO of municipal corporation, Pachayati raj: Introduction, PRI: ZilaPachayat, Elected officials and their roles, CEO Zila Pachayat: Position and role, Block level: Organizational Hierarchy (Different departments), Village level: Role of elected and appointed officials, Importance of grass root democracy.

UNIT-III

Parliamentary form of Govt. In India: President of India- Emergency provisions- National Emergency Article 352 President Rules- Article 356 Financial Emergency- Article 360 Prime Minister and Cabinet-Supreme Court of India (Indian Judiciar)

UNIT-IV

Indian Federalism: Union State relations, Legislative, Administrative and Financial relations. Lok Sabha, Rajya Sabha, Vidhan Sabha & Vidhan Parishad-Composition, Speaker, Chairman, Privileges, Legislative procedure.

UNIT-V

Parliamentary Committees: Public Accounts Committee- Estimates Committee- Committee on Public Undertakings- Election commission of India (Article -324) -Comptroller and Auditor General (CAG) of India (Article 148 to 150) Finance Commission (Article-280)-Neethi Aayog (Planning Commission) and Political Parties**.**

TEXT BOOKS

1 DD Basu-Indian Constitution
2 Dr. D. Surannaida - Indian Politica ISystem.
3 Madhav Khosla- The Indian Constitution

REFERENCES BOOKS

1. The Constitution of India. 1950 (Bare Act), Government Publication
2. M. P. Jain, Indian Constitution Law, 7th Edn, Lexis Nexis, 2014

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT
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ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – II Sem.

PHYSICAL DESIGN VERIFICATION

Subject Code: 26MVL1004	L	T	P	C
	4	0	0	4

COURSE OBJECTIVES

- To understand the VLSI design and physical design cycles, including fabrication and layout processes.
- To explore design styles and interconnect issues, focusing on noise, crosstalk, and yield.
- To study graph algorithms and data structures for solving physical design problems.
- To learn partitioning, floor planning, and routing algorithms for efficient VLSI design.
- To introduce various algorithms in physical design.

COURSE OUTCOMES

CO 1. Understand the relationship between design automation algorithms and Various
CO 2. Constraints posed by VLSI fabrication and design technology.
CO 3. Adapt the design algorithms to meet the critical design parameters.
CO 4. Identify layout optimization techniques and map them to algorithms.
CO 5. Develop proto-type EDA tool and test its efficacy

UNIT - I

VLSI Design Cycle, Physical Design Cycle, Design styles: Full Custom, Standard Cell, Gate Arrays, Field Programmable Gate Arrays, Sea of Gates and Comparison, System Packaging Styles, Multi- Chip Modules. Fabrication of VLSI circuits, Design Rules, Layout of Basic Devices, Fabrication Process and Its Impact on Physical Design, Interconnect Delay, Noise and Crosstalk, Yield and Fabrication Cost.

UNIT- II

Data Structures: Complexity Issues and NP-hardness, Basic Algorithms (Graph and Computational Geometry): Graph Search Algorithms, Spanning Tree Algorithms, Shortest Path Algorithms, Matching Algorithms, Min-Cut and Max-Cut Algorithms, Steiner Tree Algorithms.

UNIT- III

Basic Data Structures: Atomic Operations for Layout Editors, Linked List of Blocks, Bin Based Methods, Neighbor Pointers, Corner Stitching, Multi-Layer Operations. Limitations of existing Data structures.

UNIT- IV

Graph Algorithms for Physical Design: Classes of Graphs, Graphs Related to a Set of Lines, Graphs Related to a Set of Rectangles, Graph Problems in Physical Design, Algorithms for Permutation Graphs: Maximum Clique and Minimum Coloring, Maximum k-Independent Set Algorithm, Algorithms for Circle Graphs.

UNIT- V

Partitioning: Design Style Specific Partitioning Problems, Group Migrated Algorithms, Simulated Annealing and Evolution. Floor Planning and Pin Assignment, Placement and Routing Algorithms.

TEXT BOOKS

1. Naveed Shervani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.
2. Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, Handbook of Algorithms for Physical Design Automation, CRC Press, 2008.

REFERENCE BOOKS

1. "CMOS VLSI Design: A Circuits and Systems Perspective" by Neil H. E. Weste and David Harris.
2. "VLSI Physical Design: From Graph Partitioning to Timing Closure" by K. D. Meade and L. F. D. DeMicheli.

WEB LINKS

1. NPTEL Courses https://nptel.ac.in/courses/106103016

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT
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ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – II Sem.

VLSI TESTING ANDTESTABILITY

Subject Code: 26MVL1005	L	T	P	C
	4	0	0	4

COURSE OBJECTIVES

- To understand fault modeling, error diagnosis, and yield improvement in vlsi design testing.
- To learn fault simulation techniques and algorithms, including serial, parallel, and deductive methods.
- To explore test generation methods for combinational and sequential circuits, including ATPG and scan-based testing.
- To study Design for Testability (DFT) techniques and testable memory design, including BIST architectures.
- To study Testable Memory Design and System Level DFT Approaches

COURSE OUTCOMES

CO 1. Identify the significance of testable design.
CO 2. Specify fabrication defects, errors, and faults.
CO 3. Implementcombinationalandsequentialcircuittestgenerationalgorithms.
CO 4. Identify techniques to improve fault coverage.
CO 5. Analyze BIST Architectures and Testable Memory Design

UNIT-I

Role of Testing in VLSI Design Flow, Testing at Different Levels of Abstraction, Fault, Error, Defect, Diagnosis, Yield. Types of Testing, Rule of Ten, Defects in VLSI Chip. Modeling Basic Concepts, Functional Modeling at Logic Level and Register Level, Structure Models, Logic Simulation, Delay Models. Various Types of Faults, Fault Equivalence and Fault Dominance in Combinational and Sequential Circuits.

UNIT- II

Fault Simulation Applications, General Fault Simulation Algorithms: Serial and Parallel, Deductive Fault Simulation Algorithms: Two Valued deductive Fault simulation and Three Valued deductive Fault simulation.

UNIT- III

Combinational Circuit Test Generation, Structural Vs Functional Test, ATPG, Path Sensitization Methods. Difference Between Combinational and Sequential Circuit Testing, Five and Eight Valued Algebra, Scan Chain-Based Testing Method.

UNIT- IV

D-Algorithm Procedure, Problems. PODEM Algorithm, Problems on PODEM Algorithm. FAN Algorithm, Problems on FAN Algorithm. Comparison of D, FAN and PODEM Algorithms. Design for Testability, Ad-Hoc Design, Generic Scan-Based Design.

UNIT-V

Classical Scan-Based Design, System Level DFT Approaches, Test Pattern Generation for BIST, Circular BIST, BIST Architectures. Testable Memory Design: Test Algorithms, Test Generation for Embedded RAMs.

TEXT BOOKS

1. M. Abramovici, M.Breuer, and A.Friedman, “Digital Systems Testing and Testable Design, IEEE Press, 1990.
2. M.Bushnell and V.Agrawal, “Essentials of Electronic Testing for Digital, Memory & Mixed - Signal VLSI Circuits”, Kluwer Academic Publishers, 2000.

REFERENCE BOOKS

1. Stroud, “ADesigner’s Guide to Built-in Self-Test”, Kluwer Academic Publishers, 2002.
2. V.Agrawal and S.C.Seth, Test Generation for VLSI Chips, Computer Society Press.1989.

WEB LINKS

NPTELCourseshttps://archive.nptel.ac.in/courses/117/105/117105137/

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ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – II Sem.

CPLD AND FPGA ARCHITECTURES AND APPLICATIONS

Subject Code: 26MVL1006	L	T	P	C
	4	0	0	4

COURSE OBJECTIVES

- Understand the features, architectures, and applications of CPLD and FPGA devices.
- Explain the designing methods of CPLD and FPGA devices.
- Describe the architecture of the Altera MAX7000 family of CPLDs.
- Describe the architecture of the Xilinx Virtex FPGA family.
- Learn field programmable gate arrays and realization techniques.

COURSE OUT COMES

At the end of the course, the student will be able to:

CO 1. List the features and know the architecture of different PLDs.
CO 2. Design the different families of CPLD and FPGA devices.
CO 3. Realize finite state machines.
CO 4. Analyze the architecture of the Xilinx Virtex FPGA family.
CO 5. Examine the concepts of system-level design using design methods.

UNIT–I

PROGRAMMABLELOGICDEVICES:ROM,PLA,PAL,CPLD,FPGA–Features, rchitectures, Programming, Applications and Implementation ofMSI circuits using Programmable logic Devices.

UNIT–II

CPLDs: Complex Programmable Logic Devices, Altera series – Max 5000/7000 series and Altera FLEX logic-10000 series CPLD, AMD's- CPLD (Mach 1 to 5), Cypress FLASH 370 Device technology, Lattice pLSI's architectures – 3000 series – Speed performance and in system programmability.

UNIT–III

FPGAs: Field Programmable Gate Arrays- Logic blocks, routing architecture, design flow, technology mapping for FPGAs, Case studies Xilinx XC4000 & ALTERA's FLEX 8000/10000, FPGAs: AT &T ORCA's

UNIT–IV

FINITE STATE MACHINES (FSM): Top Down Design, State Transition Table, State assignments for FPGAs, Realization of state machine charts using PAL, Alternative realization for state machine charts using microprogramming, linked state machine, encoded state machine.

FSM ARCHITECTURES: Architectures Centered around non registered PLDs, Design of state machines centered around shift registers, One Hot state machine, Petrinets for state machines-Basic concepts and properties, Finite State Machine-Case study.

UNIT–V

SYSTEM LEVEL DESIGN: Controller, data path designing, Functional partition, Digital front end digital design tools for FPGAs & ASICs, System level design using mentor graphics EDA tool (FPGA Advantage), Design flow using CPLDs and FPGAs
CASE STUDIES: Design considerations using CPLDs and FPGAs of parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers.

TEXT BOOKS

1. FieldProgrammableGateArrayTechnology-S.Trimberger,Edr,1994,Kluwer Academic Publications.
2. EngineeringDigitalDesign-RICHARDF.TINDER,2nd Edition, Academic press.

REFERENCE BOOKS

1. DigitalDesignUsingFieldProgrammableGateArray,P.K.Chan&S.Mour ad,1994, Prentice Hall.
2. Field programmable gate array,S. Brown,R.J.Francis,J.Rose,Z.G.Vranesic, 2007,BSP.

WEB LINKS

1.https://www.eecg.toronto.edu/~jayar/pubs/brown/survey.pdf
2. https://www.youtube.com/watch?v=TJbI-NMJaUY

ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT
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ELECTRONICS AND COMMUNICATION ENGINEERING
M. Tech (VLSI System Design) – II Sem.

POWER MANAGEMENT IC DESIGN

Subject Code: 26MVL1E31	L	T	P	C
	3	0	0	3

COURSE OBJECTIVES

- Understand fundamentals of power management in VLSI systems.
- Analyze linear voltage regulators and LDOs.
- Explain principles of switching DC–DC converters.
- Apply systematic design methods for DC–DC converters.
- Gain awareness of emerging power management technologies.

COURSE OUTCOMES

CO 1. Explain the role of power management in VLSI systems.
CO 2. Analyze the performance of linear voltage regulators and LDOs.
CO 3. Describe the operation of switching DC–DC converters.
CO 4. Apply systematic design techniques for DC–DC converters.
CO 5. Identify emerging technologies in power management ICs.

UNIT – I

Introduction to Power Management: Need for power management, applications, power delivery in VLSI systems, discrete vs. integrated power management, types of voltage regulators (linear and switching), performance parameters such as efficiency, voltage accuracy, load and line regulation, and Point-of-Load (POL) regulators.

UNIT – II

Linear Voltage Regulators: Linear regulators and LDOs, source, sink and shunt regulators, pass transistor, error amplifier, stability and compensation techniques, PSRR, current limiting, NMOS vs. PMOS LDO regulators.

UNIT – III

Switching DC–DC Converters: Buck, Boost and Buck–Boost converters, power MOSFETs, inductor and capacitor selection, PWM modulation techniques, losses and output ripple, CCM and DCM operation, voltage-mode and current-mode control, basic compensation concepts.

UNIT – IV

Systematic Design of DC–DC Converters: Top-down design approach, topology and switching frequency selection, power MOSFET sizing and gate driver design, error amplifier and feedback network, current sensing and protection circuits, soft start, light-load operation, layout and EMI considerations.

UNIT – V

Emerging Trends in Power Management: Digitally controlled DC–DC converters, digitally controlled LDOs, dynamic voltage scaling (DVS), SIMO converters, LED driver converters, Li-ion battery charging circuits.

TEXT BOOKS

1. Switch-Mode Power Supplies: SPICE Simulations and Practical Designs, Christophe P Basso, BPB Publications, 2010.
2. Power Management Techniques for Integrated Circuit Design By Ke-Horng Chen, Wiley-Blackwell, 2016.

REFERENCE BOOKS

1. Fundamentals of Power Electronics, 2nd edition by Robert W. Erickson, Dragan Maksimovic, Springer (India) Pvt. Ltd, 2005.
2. Bernhard Wicht, Design of Power Management Integrated Circuits, Wiley, 2024.

WEB LINKS

1. NPTEL Courses (https://archive.nptel.ac.in/courses/108/106/108106159/)

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ADVANCED COMPUTER ARCHITECTURES

Subject Code: 26MVL1E32	L	T	P	C
	3	0	0	3

COURSE OBJECTIVES

- Identify the importance of architectural development tracks.
- Know the advanced processor technology and memory hierarchy technology.
- Learn multiprocessor and multi vector computers.
- Understand the linear and nonlinear scheduling processes in pipelining, various routingtechniques and message passing techniques for cache coherence problem.

COURSE OUTCOMES

After completion of this course, the students will be able to:

CO 1. Infer knowledge on Hardware and System Design concepts and gain knowledge in techniquesto enhance performance of the system.
CO 2. Understand the advanced processor technology and memory hierarchy technology.
CO 3. Understand the linear pipeline processors and know the importance of nonlinear pipelineprocessors.
CO 4. Understand the multiprocessor system interconnection, design of various network routings andthe basic concepts behind vector processing.
CO 5. Understand cache coherence problem and its solution by using protocols.

UNIT – I

Parallel Computer: State of computing, Elements of modern computer, Flynn's classification of parallel processors, System attributes to performance, Multiprocessors and Multicomputer, Shared memory multiprocessors, Distributed memory multiprocessors.

UNIT – II

Processors and Memory Hierarchy: Design space of processors, Instruction set architectures, CISC scalar processor, RISC scalar processor, Hierarchy memory technology, Inclusion Coherence and Locality.

UNIT – III

Linear and Non-Linear Pipeline Processors: Asynchronous and synchronous models, Clocking and timing control, Speedup, Efficiency and Throughput, Non-Linear Pipeline Processors-Reservation and latency analysis problems, Collision free scheduling problems, Instruction execution phases.

UNIT – IV

Multiprocessors and Multivector Computers: Inter connection structure-Crossbar switch and multiport memory, Multistage and combining network routing, Applications and drawbacks, Multivector Computers-Vector processing principles, Vector instruction types, Vector access memory schemes.

UNIT – V

Cache coherence and Synchronization Mechanisms: Cache coherence problems-Two protocol approach, Snoopy Bus Protocols, Directory Based Protocols.

Cache coherence and Message Passing Mechanisms: Message routing schemes, Deadlock and Virtual channels, Flow control strategies and Multicast routing algorithm.

TEXT BOOKS

1. "Advanced Computer Architecture-Parallelism, Scalability, Programmability" Kai Hwang and Naresh Jotwani, McGraw-Hill Publications.

REFERENCE BOOKS

1. "Computer Architecture A Quantitative Approach" 3rd edition John L. Hennessy & David A.Patterson Morgan Kaufmann.

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ASIC DESIGN

Subject Code: 26MVL1E33	L	T	P	C
	3	0	0	3

COURSE OBJECTIVES

- To understand different types of ASICs, design methodologies, and ASIC cell library architectures.
- To study programmable ASIC technologies including FPGA architectures and programmable logic cells.
- To analyze I/O cell structures, interconnect architectures, and programmable ASIC design tools.
- To apply logic synthesis techniques and low-level design entry methods in ASIC development.
- To understand simulation, timing analysis, testing methodologies, and physical design aspects of ASIC implementation.

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COURSE OUTCOMES

After successful completion of the course, the student will be able to:

CO 1. Explain ASIC types, design flow, and library-based design methodologies.
CO 2. Analyze programmable ASIC technologies including FPGA architectures and logic cell implementation.
CO 3. Design and evaluate I/O cells, interconnect strategies, and use programmable ASIC design software tools.
CO 4. Apply logic synthesis techniques and low-level hardware description methods for ASIC design optimization.
CO 5. Analyze simulation models, timing verification, testing strategies, and physical design considerations in ASIC construction.

UNIT I

INTRODUCTION TO ASICs: Types of ASICs, Design Flow, Case Study, Economics of ASICs, ASIC Cell Libraries, Transistors as resistors, Transistor Parasitic Capacitance, Logical Effort, Library Cell Design, Library Architecture, Gate-Array Design, Standard Cell Design, Data Path Cell Design.

UNIT II

PROGRAMABLE ASICS AND PROGRAMABLE ASIC LOGIC CELLS: The Anti fuse, Static RAM, EPROM and EEPROM Technology, Practical Issues,Specifications, PREDP Benchmarks, FPGA Economics, Actel ACT, Xilinx LCA, Altera Flex, Altera Max.

UNIT-III

I/O CELLS AND INTERCONNECTS & PROGRAMMABLE ASIC DESIGN SOFTWARE: DC Output, AC Output, DC input, AC input, Clock input, Power input, Xilinx I/O block, Other I/O Cells, Actel ACT, Xilinx LCA, Xilinx EPLD, Altera Max 9000, Altera FLEX, Design Systems, Logic Synthesis, The Half gate ASIC.

UNIT IV

LOW LEVEL DESIGN ENTRY AND LOGIC SYNTHESIS: Schematic Entry, Low level Design Languages, PLA Tools, EDIF, A logic synthesis example, A Comparator/MUX, Inside a Logic Synthesizer, Synthesis of Viterbi Decoder, Verilog and Logic synthesis, VHDL and Logic Synthesis, Finite State Machine Synthesis, Memory Synthesis, Optimization of the Viterbi decoder.

UNIT V

SIMULATION, TEST AND ASIC CONSTRUCTION: Types of Simulation, The Comparator/MUX Example, Logic Systems, How Logic Simulation Works, Cell Models, Delay Models, Static Timing Analysis, Formal Verification, Switch Level Simulation, Transistor Level Simulation, The importance of test, Boundary Scan Test, Faults, Faults Simulation, Automatic Test Pattern Generator, Scan Test, Built in Self-Test, A simple test Example, Physical Design, CAD Tools, System Partitioning, Estimating ASIC Size, Power Dissipation, FPGA Partitioning, Partitioning Methods.

TEXT BOOKS

1. Michael John Sebastian Smith, "Application Specific Integrated Circuits", Pearson Education, 2003.
2. L.J.Herbst, "Integrated Circuit Engineering", Oxford Science Publications, 1996.

REFERENCE BOOKS

1. Himanshu Bhatnagar, "Advanced ASIC Chip Synthesis using Synopsis Design compiler", 2nd Edition, Kluwer Academic, 2001.
2. Field programmable gate array, S. Brown, R.J. Francis, J. Rose, Z.G. Vranesic, 2007, BSP.

WEB LINKS

1.https://www.youtube.com/zerotoasic
2.https://www.youtube.com/watch?v=zd5krbQcPJw

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VLSI ARCHITECTURES

Subject Code: 26MVL1E41	L	T	P	C
	3	0	0	3

COURSE OBJECTIVES

- To design of RISC architecture and controller for a specific instruction set.
- To improve the performance of RISC processor by employing pipelining.
- To translate DSP algorithm into an efficient architecture and study the design of different building blocks of DSP architectures.
- To translate DSP algorithm into an efficient architecture and study the design of different building blocks of DSP architectures.
- To discuss pipelining and techniques to improve the performance VLSI Architectures

COURSE OUTCOMES

CO 1. Design RISC architecture and controller for a specific instruction set.
CO 2. Improve the performance of a RISC processor by employing pipelining.
CO 3. Translate DSP algorithms into efficient architectures and study the design of DSP building blocks.
CO 4. Estimate the effect of folding, unfolding, and retiming techniques on the performance of DSParchitectures.
CO 5. Explain parallel processing and techniques to improve the performance VLSI Architectures

UNIT-I

Overview of the architectures: Overview of the features of Instruction set architectures of CISC, RISC and DSP processors.CPU performance and its factors, evaluating the performance. Design of RISC processor: Building datapath and Control, multicycle implementation.

UNIT- II

Enhancing the performance with pipelining: An overview of pipelining, pipelined data path, Pipelined Control unit, various hazards of pipelining, Hazard free pipelined RISC implementation.

UNIT-III

Multiprocessors: Introduction, Multiprocessors connected by a single bus, Multiprocessors connected by a network, Network Topologies, Evolution versus revolution in Computer Architecture.

UNIT-IV

Representation of DSP Algorithms, data flow graph representations, loop bound and iterative bound, algorithms for computing iteration bound.

UNIT-V

Pipe lining and parallel processing: Introduction, pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power. Different techniques to improve the performance VLSI Architectures: Retiming, Unfolding and Folding techniques.

TEXT BOOKS

1. D.A,PattersonandJ.L.Hennessy,ComputerOrganizationandDesign:Hardware/ Software Interface, Elsevier, 2011, 4th Edition
2. Wayne Wolf, *Modern VLSI Design: System-on-Chip Design*,Pearson,4thEdition, 2009.

REFERENCE BOOKS

1. JohnL.HennessyandDavidA.Patterson, *Computer Architecture: A Quantitative Approach*, Morgan Kaufmann, 6th Edition, 2019.

2 . Keshab K. Parhi, *VLSI Digital Signal Processing Systems: Design and Implementation*, Wiley, 1999.

WEB LINKS

1. NPTELCourseswww.youtube.com/watch?v=9SnR3M3CIm4&list=PL018645397D9487AF

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IOT ARCHITECTURE AND COMPUTING

Subject Code: 26MVL1E42	L	T	P	C
	3	0	0	3

COURSE OBJECTIVES

- To introduce the fundamental concepts and architecture of Internet of Things systems.
- To understand IoT communication technologies and protocol stack.
- To study embedded computing platforms used in IoT system design.
- To analyze IoT data processing methods and cloud integration models.
- To explore real-world IoT applications and understand basic security mechanisms.

COURSE OUTCOMES

After successful completion of the course, students will be able to:

CO 1. Explain the architecture, components, and functional blocks of IoT systems.
CO 2. Describe IoT communication technologies and analyze basic IoT protocols.
CO 3. Design simple IoT systems using embedded platforms such as Arduino and Raspberry Pi.
CO 4. Demonstrate understanding of IoT data processing and cloud integration.
CO 5. Identify security challenges and evaluate IoT applications in various domains.

UNIT – I

Fundamentals of IoT Architecture: Evolution and concept of Internet of Things, Characteristics of IoT, Basic IoT Architecture (3-layer and 5-layer models), Functional blocks of IoT system, Sensors, Actuators and Smart Objects, Introduction to Edge, Fog and Cloud in IoT.

UNIT – II

IoT Communication Technologies Basics of networking for IoT, IEEE 802.15.4 and Wi-Fi (overview), LoRa WAN (basic concept), IPv4 and IPv6 basics, 6LoWPAN, Application layer protocols: MQTT and CoAP.

UNIT – III

IoT Embedded Platforms and System Design IoT system design methodology, Embedded computing basics, Microcontrollers and SoC (overview), Arduino programming and sensor interfacing, Raspberry Pi basics and Python programming, Simple IoT system implementation.

UNIT – IV

IoT Data Processing and Cloud Integration Types of IoT data (structured/unstructured), Data storage basics, Introduction to Cloud computing, AWS IoT (basic architecture), Edge data processing concept, Introduction to Machine Learning in IoT.

UNIT – V

IoT Applications and Security issues in IoT (basic concepts), Authentication and encryption basics, Smart Home, Smart Cities, Smart Agriculture, Healthcare IoT, Industrial IoT overview.

TEXTBOOKS

1. IoT Fundamentals: Networking Technologies, Protocols and Use Cases for Internet of Things, David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Rob Barton and Jerome Henry, Cisco Press, 2017.
2. Internet of Things – A hands-on approach, Arshdeep Bahga, Vijay Madisetti, Universities Press, 2015

REFERENCE BOOKS

1. The Internet of Things – Key applications and Protocols, Olivier Hersent, David Boswarthick, Omar Elloumi and Wiley, 2012.
2. “From Machine-to-Machine to the Internet of Things – Introduction to a New Age of Intelligence”, Jan Ho¨ ller, Vlasios Tsiatsis, Catherine Mulligan, Stamatis, Karnouskos, Stefan Avesand. David Boyle and Elsevier, 2014.

WEB LINKS

1.https://www.youtube.com/watch?v=pS_w1KG2cPw
2.https://www.youtube.com/watch?v=JC3cQ2MB_34

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RELIABILITY OF DEVICES AND CIRCUITS

Subject Code: 26MVL1E43	L	T	P	C
	3	0	0	3

COURSE OBJECTIVES

- Understand fundamental concepts of reliability and failure mechanisms in electronic systems.
- Apply mathematical and statistical models for reliability analysis.
- Analyze physics-of-failure mechanisms affecting semiconductor devices.
- Evaluate circuit performance degradation due to reliability issues.
- Understand packaging-related reliability concerns in VLSI systems.

COURSE OUTCOMES

CO 1. Explain fundamental reliability concepts and measures used in electronic systems.
CO 2. Apply statistical reliability models to analyze failure behavior.
CO 3. Identify and analyze physics-of-failure mechanisms in semiconductor devices.
CO 4. Evaluate the impact of reliability issues on circuit performance.
CO 5. Understand packaging-related reliability challenges in VLSI systems.

UNIT - I

Fundamentals of Reliability Engineering: Definitions of reliability, failure, failure modes and mechanisms, basic reliability concepts, reliability functions and relationships, bathtub curve, exponential failure density and distribution, mean, standard deviation, reliability measures such as MTTF, MTTR, and MTBF.

UNIT – II

Mathematical Models for Reliability Analysis: Failure rates, normal distribution, Six Sigma , exponential distribution, Weibull and lognormal distributions for reliability modeling, manufacturing yield concepts.

UNIT – III

Physics of Failure in Semiconductor Devices:
Mass transport-induced failures including electro migration and stress voiding, electronic charge-induced failures such as dielectric breakdown, hot carrier effects, electrical overstress (EOS) and electrostatic discharge (ESD), environmental damage due to moisture ingress, corrosion and radiation effects.

UNIT – IV

Reliability Impact on Circuit Performance: Circuit performance degradation due to NBTI and PBTI, oxide breakdown, random telegraph noise (RTN), radiation damage, impact of parasitic effects, process and temperature variations, and electromagnetic compatibility (EMC), electromagnetic interference (EMI), and ESD considerations.

UNIT – V

Packaging and Interconnect Reliability: Introduction to semiconductor device packaging, packaging materials and processes, stresses induced due to packaging, degradation of interconnect such as solder creep and fatigue.

TEXT BOOKS

1. M. Ohring, Reliability and Failure of Electronic Materials and Devices, First Edition, Academic Press, 1998, 2nd Edition
2. J.W. McPherson, Reliability Physics and Engineering, Second Edition, Springer, 2013, 2nd Edition

REFERENCE BOOKS

1. Yuan Taur and T. Ning, "Fundamentals of Modern VLSI Devices," Cambridge University Press, 1998.
2. J.Ross, Microelectronic Failure Analysis, Sixth Edition, ASTM International, 2011.

WEB LINKS

1. NPTEL Courses (https://nptel.ac.in/courses/112105267).

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PHYSICAL DESIGN VERIFICATION LAB

Subject Code: 26MVL1103	L	T	P	C
	0	0	4	2

COURSE OBJECTIVES

- To understand and implement graph-based algorithms for solving connectivity, routing, and optimization problems in VLSI physical design.
- To apply minimum spanning tree, shortest path, and Steiner tree algorithms for efficient global routing and wire length minimization.
- To design and analyze circuit partitioning techniques including Kernighan–Lin, Fiduccia–Mattheyses, and simulated annealing for performance optimization.
- To develop and optimize floor planning strategies using constraint-based, integer programming, and rectangular dualization approaches.
- To implement routing algorithms such as maze routing, line-probe routing, and two-terminal shortest path methods using C/C++.

COURSE OUTCOMES

Upon successful completion of the lab, students will be able to:

CO 1. Analyze and implement graph traversal, MST, and shortest path algorithms for layout connectivity and timing optimization in VLSI systems.
CO 2. Apply Steiner tree and global routing techniques to minimize interconnect wire length and improve routing efficiency.
CO 3. Design and evaluate circuit partitioning algorithms (KL, FM) for balanced and Performance - aware VLSI design.
CO 4. Develop optimized floor planning solutions using constraint-based models, integer programming, and rectangular dualization techniques.
CO 5. Implement and validate routing strategies including maze routing and line-probe routing for efficient IC layout realization.

CYCLE-1

1. Graph algorithms:
2. Graph search algorithms:
3. Depth first search
4. Breadth first search
5. Spanning tree algorithm:
6. Kruskal’s algorithm
7. Shortest path algorithm:
8. Dijkstra algorithm
9. Floyd-Warshall algorithm
10. Steiner tree algorithm

CYCLE-2

1. **Partitioning algorithms:**
    a. Kernighan–Linalgorithm
    b. Fiduccias–Mattheyses algorithm
    c. Simulated annealing and evolution algorithms

2. **Floor planning algorithms:**
    a. Constraint based methods
    b. Integer programming-based methods
    c. Rectangular dualization based methods
    d. Simulated evolution algorithms

3. **Routing algorithms –Two terminal algorithms:**
    a. Maze routing algorithms:
    b. Lee's algorithm
    c. Soukup's algorithm
    d. Hadlock algorithm
    e. Line-Probe algorithm
    f. Shortest path-based algorithm

Software required: C/C++ Programming Language/ Relevant software.

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M. Tech (VLSI System Design) – II Sem.

RESEARCH METHODOLOGY AND IPR

Subject Code: 26MCC1001	L	T	P	C
	2	0	0	2

COURSE OBJECTIVES

- Formulate research problems with clarity and develop strong analytical skills.
- Apply structured research methodology, literature review techniques, and ethical practices to academic work.
- Interpret research data effectively and master the mechanics of technical report writing.
- Gain a comprehensive understanding of Intellectual Property Rights (IPR) and the legalities of the patenting process.
- Understand the global landscape of patent rights, technology transfer, and emerging trends in IP.

COURSE OUTCOMES

CO 1. Summarize the fundamental concepts, types, and systematic processes of scientific research.
CO 2. Formulate a well-defined research problem by applying systematic selection techniques
CO 3. Construct a comprehensive literature review and theoretical framework while maintaining high ethical standards.
CO 4. Execute data interpretation and produce high-quality technical reports and oral presentations.
CO 5. Navigate the legalities of Intellectual Property Rights, including patent filing, licensing, and emerging IP trends.

UNIT-I

Introduction to Research Methodology: Meaning, objectives, and motivation in research.Research Taxonomy: Types of research (Descriptive vs. Analytical, Applied vs. Fundamental, and Quantitative vs. Qualitative). Methodology: Research approaches, significance of research, and the distinction between Research Methods vs. Methodology. Scientific Rigor: Research and the scientific method; Importance of understanding the research process from inception to completion.

UNIT-II

Defining the Research Problem: Quality Standards: Criteria of good research; Common problems encountered by researchers in India. Problem Formulation: The art of defining the research problem; Necessity and importance of a well-defined problem. Techniques: Step-by-step process of identifying and selecting a research problem. Application: Practical illustrations and the logic of narrowing down a broad area into a researchable topic.

UNIT-III

Literature Review and Research Ethics: Strategic Review: Place of literature review in research; Bringing clarity and focus to the problem; improving methodology and broadening knowledge base. Execution: Searching existing literature, reviewing selected literature, and contextualizing findings. Frameworks: Developing theoretical and conceptual frameworks for the study.Integrity: Writing about the literature reviewed; Analysis of Plagiarism and adherence to Research Ethics.

UNIT-IV

Interpretation and Report Writing: Data Synthesis: Meaning and techniques of interpretation; Precautions to take during data interpretation. Technical Communication: Significance of report writing; Different steps and layout of a formal research report. Formatting & Mechanics: Types of reports, oral presentation skills, and the mechanics of writing a research report. Quality Control: Precautions for writing effective and accurate research reports.

UNIT-V

Nature of Intellectual Property and Patenting: IP Fundamentals: Nature of Intellectual Property: Patents, Designs, Trademarks, and Copyrights. The Patent Lifecycle: From technological research and innovation to development; Procedure for grant of patents. Global Framework: International cooperation on IP; Patenting under the Patent Cooperation Treaty (PCT). Rights & Trends: Scope of patent rights; Licensing and transfer of technology; Patent databases. Emerging Areas: Geographical Indications (GI), Traditional knowledge case studies.

TEXT BOOKS

1. Kothari, C. R(1990). Research methodology, 2nd edition, New Age International Publishers.
2. Kothari, C. R., & Garg, G. (2024). Research methodology: Methods and techniques (5th ed.). New Age International Publishers.
3. Ramappa, T. (2021). Intellectual property rights under WTO (3rd ed.). S. Chand Publishing.

REFERENCE BOOKS

1 Chawla, D.,⌊ & Sondhi, N. (2016). Research methodology: Concepts and cases (2nd ed.) Vikas Publishing House.
2. Cornish, W., Llewelyn, D.,⌊ & Aplin, J. (2025). Intellectual property: Patents, copyright, trade marks and allied rights (10th South Asian ed.).Sweet & Maxwell. Available at Bharat Law House.
3. Controller General of Patents, Designs and Trade Marks. (2024). Manual of patent practice⌊ and procedure. IP India Official Website.
4. World Intellectual Property Organization. (2024).PCT –The International Patent⌊ System. WIPO