

LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
1	2/7/12	Number systems Introduction	I	(Black Board) BB		
2	3/7/12	Binary, octal		BB		
		Decimal & Hexadecimal		BB		
		number systems		BB		
3	5/7/12	Conversion of numbers		BB		
4	6/7/12	from one radix to		BB		
		another radix.		BB		
5	6/7/12	x 's Complement &		BB		
6	7/7/12	$(x-1)$'s Complement		BB		
7	9/7/12	Subtraction of		BB		
		unsigned numbers.		BB		
8	10/7/12	problems.		BB		
9	12/7/12	Signed Binary numbers.		BB		
10	13/7/12	weighted codes.		BB		
		non-weighted codes		BB		
11	13/7/12	problems		BB		
12	14/7/12	problems.		BB		
13	16/7/12	Introduction.	II	BB		

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		NOT, AND, OR gates		BB		
15	19/7/12	Boolean theorems		BB		
16	20/7/12	Complement and Dual of logic expressions.		BB		
17	21/7/12	Universal gates		BB		
		EX-OR & EX-NOR gates		BB		
18	23/7/12	Tutorial				
19	24/7/12	Sum-of-products		BB		
		Product-of-sums		BB		
20	26/7/12	Minimization of Logic Functions		BB		
21	27/7/12	Two level realization of logic functions		BB		
22	28/7/12	Verilog programming for minimized logic functions		BB		
23	30/7/12	problems (Tutorial)		BB		
24	31/7/12	Introduction	III	BB		
25	2/8/12	Karnaugh Map		BB		

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26	3/8/12	Two Variable Minimization		BB		
27	4/8/12	Three Variable Minimization		BB		
28	6/8/12	Four variable "		BB		
29	7/8/12	POS & SOP		BB		
30	9/8/12	Simplification with Don't Care Conditions		BB		
31	10/8/12	using K-Map		BB		
32	11/8/12	problems		BB		
33	13/8/12	Tutorial on unit-IV		BB		
34	14/8/12	Introduction.	IV	BB		
35	16/8/12	Design of Half Adder.		BB		
36	17/8/12	Design of Full Adder		BB		
37	18/8/12	Half Subtractor Full Subtractor		BB		
38	20/8/12 (T)	Ripple Adders & Subtractor		BB		
39	21/8/12	Ripple Adders & Subtractor Using 1's & 2's Comp method		BB		
40	23/8/12	Serial Adder		BB		
41	25/8/12	Carry Look Ahead Adder.		BB		

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42	3/9/12 (T)	Introduction	<u>V</u>	BB		
43	4/9/12	Design of Decoders		BB		
44	6/9/12	Multiplexers		BB		
		Demultiplexers				
45	7/9/12	Higher order Multiplexer & Demultiplexer		BB		
46	8/9/12	Realization of Boolean functions using decoders & Multiplexers.		BB		
47	10/9/12 (T)	Tutorial.		BB		
48	11/9/12	priority Encoder		BB		
49	13/9/12	Code Converters.		BB		
50	14/9/12	Design problems.		BB		
51	15/9/12	Magnitude Comparator		BB		
52	17/9/12 (T)	Tutorial		BB		
53	18/9/12	Introduction	<u>VI</u>	BB		
54	20/9/12	programmable logic Array.		BB		
55	21/9/12	programmable Array logic		BB		

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56	22/9/12	PROM		BB		
57	24/9/12	Tutorial		BB		
58	25/9/12	Realization of		BB		
59	27/9/12	Switching Functions using PROM, PLA & PAL		BB		
60	28/9/12	Comparison of PROM, PLA & PAL		BB		
61	29/9/12	Design problems		BB		
62	22/9/12	Tutorial		BB		
63	23/9/12	Introduction	VII	BB		
64	25/9/12	Classification of seq lfts		BB		
65	26/9/12	Latch & Flipflop		BB		
66	27/9/12	RS latch using NAND & NOR gates		BB		
67	29/9/12	Tutorial		BB		
68	30/9/12	RS, JK, T &		BB		
69	1/10/12	DE flipflops		BB		
70	2/10/12	Truth & Excitation tables		BB		

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71	4/10/12	Conversion of Flipflops		BB		
72	5/10/12	flipflop with		BB		
73	6/10/12	Asynchronous inputs.		BB		
74	8/10/12	Tutorial		BB		
75	11/10/12	Introduction	VIII	BB		
76	12/10/12	Design of Registers		BB		
77	13/10/12	Buffer & Control		BB		
		Buffer Registers		BB		
78	15/10/12	Tutorial		BB		
79	18/10/12	Bidirection & USR		BB		
80	19/10/12	Design of Ripple		BB		
		Counters, Ring Counters				
81	20/10/12	Synchronous Counters		BB		
82	22/10/12	Tutorial		BB		
83	23/10/12	Johnson Counter		BB		
84	25/10/12	Revision		BB		
85	26/10/12	Revision		BB		
86	27/10/12	Revision.		BB		