LESSION PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
1	2/7	Introduction to Number system	I			
2	2/7	Binary, octal, Decimal Hexadecimal Numbersyste				
4	4/7	conversion of numbers from one radix to another				
5	4/7	r's complement				
6	5/7	(r-1)'s complement				
7	9/7	Subtraction of unsigned numbers				
8	11/7	problems				
9	12/7	signed binary numbers				
11	17/7	weighted & non weighted codes				
12	16/7	Basic gates NOT, AND, OR	II			
13	16/7	Boolean theorems				
14	18/7	complement & dual of logical Expressions				
15	21/7	universal gates				
17	25/7	Ex-OR, Ex-NOR, SOP, POS				
18	26/7	Minimization of logic functions using Boolean theore				
20	27/7	Two level realization of logic functions using universal gates				
21	30/7	verilog programming				
22	30/7 2228	for the minimized logic function				

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
23	4/8	Karnaugh Map Method (K-map)	III			
26	6/8 & 8/8	Minimization of boolean functions upto 4 Variable				
28	9/8	POS & SOP				
30	9/8 11/8	Simplifications with don't care conditions				
31	11/8	Design of Half adder	IV			
22	13/8	Full adder				
33	15/8	Half Subtractor				
34	16/8	Full Subtractor				
35	16/8	Ripple adder & Subtractors				
36	16/8	using one's & Two's complement method				
37	27/8	Serial adder				
38	22/8	carry look ahead adder				
39	25/8	Design of decoders	V			
40	3/9	encoders				
41	3/9	Multiplexers				
42	3/9	Demultiplexers				
43	5/9	Higher order demultiplexer & multiplexers				

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
46	6/9 & 8/9	priority encoder				
47	8/9	code converters				
49	8/9 & 10/9	Magnitude comparator				
50	12/9	Problems				
51	12/9	PLA	VI			
52	13/9	PAL				
53	15/9	PROM				
54	15/9	Realization of switching functions using PROM, PAL, PLA				
55	15/9	comparisons				
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57	17/9 & 20/9	classification of sequential circuits	VII			
58	22/9	Basic sequential logic circuits				
59	24/9	Latches & flipflops				
60	27/9	RS latch using NAND & NOR gates				
62	23/10 & 1/10	Truth tables				
63	3/10	RS, JK, T and D flipflops				
64	4/10	Truth & Excitation tables				
66	4/10 & 6/10	conversion of flipflop				
68	8/10	Flipflops with Asynchronous inputs				

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
68	11/10	Design of registers	VIII			
69	13/10	Buffer registers				
70	13/10	control buffer registers				
72	15/10	Bidirectional shift registers				
73	17/10	unidirectional shift registers				
74	17/10	Design of ripple counters				
75	17/10	Synchronous counters				
76	18/10	variable Modules counters				
77	20/10	Ring counters				
78	25/10	Johnson counters				