

**ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT
(AN AUTONOMOUS INSTITUTION)**

EXAMINATION BRANCH

I M. TECH - I SEMESTER – (AR13 REGULATION) 2014 BATCH (AUTONOMOUS)

I MID EXAMINATIONS, JANUARY-2015

T I M E T A B L E

Examination Timings 02.00 PM to 04.00 PM

Date & Day of Examination	TE	DECS	IT	PEED	VLSI System Design	CSE
05-01-2015 (MONDAY)	Optimization Techniques & Applications	Digital System Design	Advanced Data Structures	Electrical Machine Modeling & Analysis	Digital System Design	Data Structures & Algorithms
06-01-2015 (TUESDAY)	Advanced Thermodynamics	VLSI Technology & Design	Advanced Unix Programming Data Structures	Analysis of Power Electronic Converters	VLSI Technology & Design	Computer Organization and Architecture
07-01-2015 (WEDNESDAY)	Advanced Heat & Mass Transfer	Analog & Digital IC Design	Data Base Management Systems	Power Electronic Control of DC Drives	Analog & Digital IC Design	Database Management Systems
08-01-2015 (THURSDAY)	Advanced Fluid Mechanics	Detection and Estimation of Signals	Advanced Computer Network	Micro Controllers & Applications	VHDL Modeling of Digital Systems	Software Engineering
09-01-2015 (FRIDAY)	Solar Energy Technology	Embedded & Real Time Systems	Code Optimization	Modern Control Theory	Embedded & Real Time Systems	Operating Systems
10-01-2015 (SATURDAY)	Non Conventional Energy Sources	Advanced Digital Signal Processing	Object Oriented Software Engineering	Non Conventional Energy Sources and Applications	Electronic Design Automation Tools	Object Oriented Programming

**Copy to: Director / Principal / Controller of the Examinations / HODs / Officer I/c, Examinations,
Estate Officer / In-charge, Transport**

KB Madhu Sahu

PRINCIPAL

17-12-2014